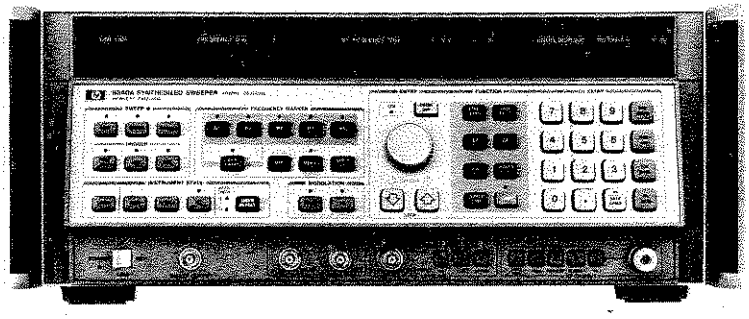
OPERATING AND SERVICE MANUAL

8340A SYNTHESIZED SWEEPER

10 MHz to 26.5 GHz



Preliminary Manual

HEWLETT PACKARD

SAFETY CONSIDERATIONS

GENERAL

This product and related documentation must be reviewed for familiarization with safety markings and instructions before operation. This product has been designed and tested in accordance with international standards.

SAFETY SYMBOLS

Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual (refer to Table of Contents).

Indicates hazardous voltages.

Indicates earth (ground) terminal.

WARNING The WARNING sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in personal injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

CAUTION The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood and met.

SAFETY EARTH GROUND

This is a Safety Class I product (provided with a protective earthing terminal). An uninterruptible safety earth ground must be provided from the main power source to the product input wiring terminals, power cord, or supplied power cord set. Whenever it is likely that the protection has been impaired, the product must be made inoperative and be secured against any unintended operation.

BEFORE APPLYING POWER

Verify that the product is configured to match the available main power source per the input power configuration instructions provided in this manual.

If this product is to be energized via an autotransformer make sure the common terminal is connected to the neutral (grounded side of mains supply).

SERVICING

WARNING

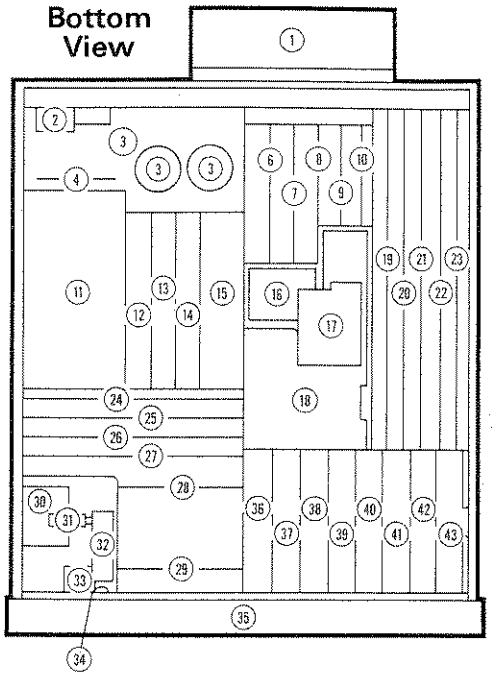
Any servicing, adjustment, maintenance, or repair of this product must be performed only by qualified personnel.

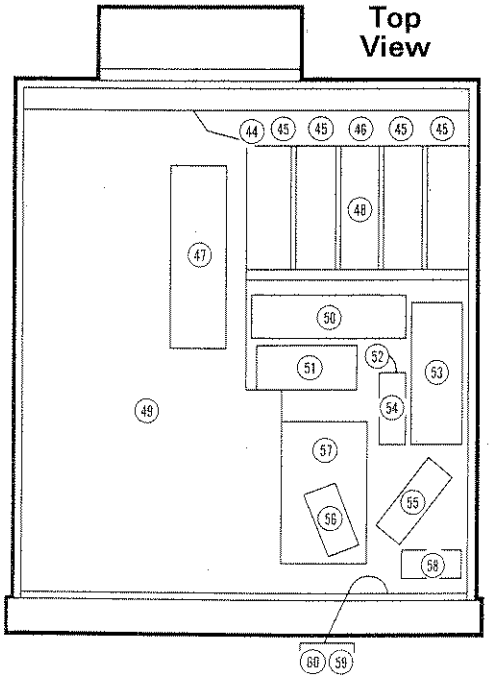
Adjustments described in this manual may be performed with power supplied to the product while protective covers are removed. Energy available at many points may, if contacted, result in personal injury.

Capacitors inside this product may still be charged even when disconnected from its power source.

To avoid a fire hazard, only fuses with the required current rating and of the specified type (normal blow, time delay, etc.) are to be used for replacement.

REFERENCE GUIDE TO SERVICE DOCUMENTATION





Assy./Ref. Des.	Description	Location	Volume 2: Ref.-M/N Loops	Volume 2: 20/30 Loops	Volume 2: Swp. Gen.-YO Loop	Volume 2: Motherboard	Volume 2: Controller	Volume 3: Front/Rear Panel	Volume 3: RF Section	Volume 3: Power Supplies
A1	Alpha Display	35					●			
A2	Display Driver	35					●			
A3	Display Processor	35					●			
A4	Not Assigned	-								
A5	Keyboard	35					●			
A6	Keyboard Interface	35					●			
A7	Lower Keyboard	35					●			
A8	3.7 GHz Oscillator	57						●		
A9	Band 0 Pulse Modulator	56						●		
A10	Directional Coupler	32						●		
A11	Band 1-4 Detector	31						●		
A12	Band 0 Detector	34						●		
A13	SYTM (Switched YIG Tuned Multiplier)	36						●		
A14	Band 1-4 Power Amplifier	53						●		
A15	Band 0 Low Pass Filter	52						●		
A16	Band 1-4 Modulator/Splitter	51						●		
A17	Band 0 Mixer	54						●		
A18	Band 0 Power Amplifier	55						●		
A18A2	Band 0 Splitter	60						●		
A19	Capacitor Assembly	48							●	
A20	RF Section Filter	50						●		
A21	Pulse Modulator Driver	28						●		
A22	Not Assigned	-								
A23	Not Assigned	-								
A24	Attenuator Driver/SRD Bias	28						●		
A25	ALC Detector	27						●		
A26	Linear Modulator	26						●		
A27	Level Control	25						●		
A28	SYTM Driver	24						●		
A29	Reference Phase Detector	12	●							
A30	100 MHz VCXO (Voltage Controlled Crystal Osc.)	13	●							
A31	M/N Phase Detector	14	●							
A32	M/N VCO (Voltage Controlled Osc.)	15	●							
A33	M/N Output	15	●							
A34	Reference-M/N Motherboard	5	●							
A35	Rectifier	4							●	
A36	PLL1 VCO (Voltage Controlled Osc.)	36		●						
A37	PLL1 Divider	37		●						
A38	PLL1 IF	38		●						
A39	PLL3 Upconverter	39		●						
A40	PLL2 VCO (Voltage Controlled Osc.)	40		●						
A41	PLL2 Phase Detector	41		●						
A42	PLL2 Divider	42		●						
A43	PLL2 Discriminator	43		●						
A44	YIG Oscillator (YO)	18			●					
A45	Pre-Leveler	18			●					
A46	7 GHz Low Pass Filter	18			●					
A47	Sense Resistor Assembly (YO circuit)	47			●					
	(STYM circuit)	47						●		
A48	YO Loop Sampler	18			●					
A49	YO Loop Phase/Detector	18			●					
A50	YO Loop Interconnect	17			●					
A51	Reference Oscillator	16	●							
A52	Positive Resulator	6							●	
A53	Negative Regulator	7							●	
A54	YO Pretune DAC/Delay Compensation	8			●					
A55	YO Driver	9			●					
A56	-15V Regulator	10							●	
A57	Marker/Bandcross	19				●				
A58	Sweep Generator	20			●					
A59	Digital Interface	21				●				
A60	Processor	22				●				
A61	Memory	23				●				
A62	Main Motherboard	49				●				
A63	70 dB RF Attenuator	59						●		
AT1	Peripheral Mode Isolator	58						●		
B1	Fan Assembly	1							●	
A62C1-3	Power Supply Filter Capacitors	3							●	
FL1	AC Line Module	2							●	
A62Q1-4	Power Supply Regulating Transistors	2							●	
A62S1	Power Supply Thermal Switch	44							●	
T1	Power Supply Transformer	11							●	
A62U1	Power Supply Regulator	46							●	

CONTROLLER SECTION

A57 MARKER BANDCROSS ASSEMBLY, CIRCUIT DESCRIPTION

Introduction

The Marker Bandcross board generates the Z-axis intensification signal required to place intensity markers on a CRT. If enabled by the front panel, amplitude markers will be generated by sending a marker signal to the leveling circuits. The same circuits that detect markers are used to detect band crossings or the end of sweep. These circuits will cause the sweep to be stopped and the microprocessor to be activated. Other circuits interface with rear panel interface connections. Hardware on this board is used during self test to verify the operation of the 16 bit microprocessor data bus.

Sweep Event Detection (Blocks A, B, C, D, E, And F)

A sweep event is a MARKER, a BAND CROSSING or the END OF SWEEP. Prior to the beginning of a sweep, the microprocessor will Store in the Sweep Event Memory (Block B) a series of numbers which correspond to all the sweep events that are to take place during a sweep. These numbers are loaded in the following manner:

1. The Processor Sets Address Register (Block A) to 0 (i.e., sets DB0-6 to zero then outputs address 12,R3:)

2. The Processor writes into the Sweep Event Memory (Block B) a series of numbers corresponding to the sweep events. NOTE: The Address Register is automatically incremented after each write to memory (address 12,R0: to U1 pin 5).

3. The Processor Sets the Address Register back to 0.

Before a sweep begins, the processor determines how many sweep events their will be in the sweep. For example, for a sweep containing one Bandcrossing and a Marker, there would be 4 sweep events, two for the marker, one for the the bandcrossing, and one for the end of sweep. The processor then computes at what point in the sweep each event occures and converts this information to a number from 0-999 which would correspond to the 0-10V sweep. This series of numbers are written into the Sweep Event Memory via B0-B9. When the Address Register (Block A) is set to location 0, the first number stored in the memory appears at the input of the sweep comparitor DAC U3. The DAC converts this number to a voltage between 0-10V. This voltage is not available at the the output of U3 but is compared internally to the MARKER RMP (0-10V) signal. When the MARKR RAMP rises to a voltage equal the value the DAC is set to, the output of U3 (Pin 15) will fire the comparitor U6 and the 1st sweep event occurs. This causes the MARKER and the BANDCROSS flip flops to be clocked. The data

stored in the flip flops and taken from data bits 10 and 11 of the RAM will determine what kind of sweep event has occured. MARKERS: A marker is created by two sweep EVENTS. The first EVENT turns the marker ON the SECOND turns the marker OFF. Markers are 1/1000 of the DISPLAY wide. When a user attempts to change one of the frequency parameters in the middle of a slow sweep (300 mS or longer) the SWEEP EVENT DETECTION circuitry is used to determine the position that the sweep is at allowing the instrument to phaselock to a frequency appropriate to the current sweep position. For faster sweep times, the instrument will defer making frequency changes until the beginning of the next sweep.

Address Register A

U1 and U10 comprise a 6 bit counter register. The counter is preset when the microprocessor writes to I/O address 12,R3: via pin 11. The Address Register can be counted or incremented two ways: First by the MicroProcessor writing to I/O address 12,R0:, and secondly when Timer U5B (Block E) fires. The signal from U5B indicates that a sweep event has occured and that the SWEEP EVENT DETECTION circuitry should get ready for the next sweep event. The outputs of the Address Register (A0 through A6) are used to address the Sweep Event Memory (Block B).

Sweep Event Memory B

U2 and U15 are RAMs each containing 128 8 bit bytes. They are combined to provide 128 16 bit words of memory. Sweep events are stored into the RAM when the microprocessor does a write to I/O address 12,R0:. U8 and U16 (Block C) are buffers through which the microprocessor reads or writes RAM data. The RAM is addressed by the Address Register (Block A). In normal operation of the instrument only about 15 of the 128 words of RAM are used. Each location used corresponds to a single sweep event that is to occur during the sweep. The RAM has stored in it, the position along the sweep where each event is to occur, as well as informaton indicating what kind of sweep event each one is.

Read/Write RAM Buffer C

U8 and U16 make a 16 bit bidirectional buffer which connects the microprocessor with the Sweep Event Memory (Block B). When the microprocessor sends I/O Address 12,R0:, the buffer transfers data from the instrument data bus (DB0 thru DB15) to B0 thru B15. When the microprocessor sends I/O Address 12,R2: data is transfered the opposite direction (i.e., from the Sweep Event Memory to the microprocessor).

Sweep Comparitor D

U3 is a 10 bit DAC which compares the 0 - 10V MARKER RMP to the binary number placed at its input by the Sweep Event Memory (Block B). The MARKER RMP (0-10V) is connected to the V-Feedback input of U3 (Pin 16). At tge beginning of a sweep the output of the DAC will be below 0 volts. When the voltage applied by the MARKER RMP (0-10V) is equal to the corresponding digital number at the DAC's input will go above 0 volts. Comparitor U6 is set to trip when the output of the DAC rises above 0 volts. For example if a Sweep Event is to occure at mid sweep, the following conditions would exist: The DAC would have the number 500 decimal or 111110100 binary placed at its digital input. Before the Marker Ramp gets to 5 volts, which represents the exact middle of the sweep, the DAC output would be below 0 Volts and the Comparitor output (Pin 7) would be LOW. As the MARKER RMP approaches 5 volts, the output of the DAC would approach 0 volts. When it gets to 0 volts the comparitor will fire causing its output to go HIGH. When the comparitor fires, R28, R26 and R27 cause a 2mV offset to be made to the positive input of the comparitor (Pin 2). This insures that the comparitor having just fired will not change states due to noise on the MARKER RMP. R32 (10V END of SWEEP ADJ.) is adjusted to make the end of sweep voltage equal 10.000 V.

RAM DATA UNSTABLE TIMER E

This circuit debounces the output of the SWEEP COMPARITOR (Block D) and causes the ADDRESS REGISTER (Block A) to be incremented after each sweep event has been detected. U5B is triggered by the comparitor firing and outputs a 700 nS pulse. The pulse sets timmer U5A and also clocks the Marker/Bandcross Flip-Flops (Block F). Timer U5A will reset after 5.7 uS and is used to keep Timer U5B from being fired again until the circuits in Blocks A,B,C and D have had time to settle following a sweep event. U20B controls the reset input of Timer U5B. The inputs of U20B are used to disable the timmer. Pin 5 of U20B is connected to U12B pin 6 (Block M) and is HIGH when the sweep has been stopped. This keeps the timmer from firing after the sweep has been stopped. n Pin 6 of U20B is controlled by the microprocessor thru register U18 (Block L). This is set HIGH to disable the timmer when the instrument does its self test.

Marker/Bandcross Flip-Flops F

U11B and U11A are used to store B10 and B11 from the Sweep Event Memory (Block B). These two signals indicate what kind of sweep event is to take place. Bit 10 is connected to U11B Pin 12 and sets the state of the MKR control line connected to its output (Pin 5). When a Bandcrossing occurs the sweep will be stopped so

that the microprocessor can initiate phaselock for that bandcrossing. This is done by the LBX signal. When a Marker occurs, the sweep is not stopped and the marker is generated as the sweep progresses.

Manual Sweep DAC G

The manual sweep DAC U4 is used only in MANUAL SWEEP mode. A binary number between 0-1000 is written to the DAC. The digital input of the DAC is connected to registers U9 and U17. The microprocessor is connected to U9 and U17 via the I/O Data Buss. Data is clocked into these registers by strobe 13,R2: (Block K). In MANUAL SWEEP mode the MKR RAMP should always be at 0 volts. The DAC converts its digital input to a voltage (0 to -10 V) at its output Pin 15. The Op Amp U7 will invert this to provide the 0 to +10V SWEEP OUT at TP5.

The SWEEP OUT of Block G (U7 Pin 6) is the result of either the manual sweep DAC U4 when MANUAL SWEEP mode is selected or the MKR RAMP when MANUAL SWEEP is not selected.

When the instrument is not in MANUAL SWEEP mode the input of the DAC is set to 0 by the microprocessor and the MKR RAMP is simply buffered by Op Amp U7. .

THE MANUAL GAIN adjustment R33 is adjusted to obtain 10.000V at the sweep output when in MANUAL SWEEP and the manual frequency is set to the maximum possible value for a given sweep. For example: Set R33 to obtain 10.000V at TP4 when MANUAL SWEEP is ON and the RPG has been turned clockwise until the manual frequency is equal to the STOP frequency.

Sweep Outputs H

The SWEEP OUT is buffered by U30 and U27 which are connected to the front and rear panel Sweep Output connectors. Floating grounds are needed to eliminate ground loops which would cause 60Hz signals to appear on the sweep outputs. The front and rear panel sweep output connectors are floating. Any low frequency noise found on the floating front or rear panel sweep output connectors is connected by the RTN lines to the non inverting inputs of the buffer Op Amps. This allows the Op Amps to sense and remove this unwanted noise. L4-L7 and C21-C22 are provided to eliminate high frequecy noise.

Read Status Buffer I

Buffer U24 enables the processor to monitor the state of the following signals by doing a read from I/O address 12,R1:.

1. The SWEEP COMPARITOR (Pin 12)

2. The MARKER flip flop (Pin 14)

3. The HSP line (Pin 2)

Control Register J

Register U23 enables the processor to directly control the state of the various interface lines connected to the register. This is done when the microprocessor writes data to I/O address 13,R3:. The data is then available continuously at the output of the register.

AND gate U29A is used to control the RF MARKER signal. When HIGH this signal causes the RF POWER CONTROL circuits to slightly increase the RF power. This is used as a marker. U29A pin 1 is used to turn this feature on or off.

Micro Processor Read And Write Strobes K

The instrument processor outputs I/O address information on the I/O Address Bus (ADR0 thru ADR4 plus ADR5 which becomes SIOA). U28 decodes the address and generates the appropriate strobe:

These strobes are used throughout this assembly to either clock registers causing them to store data found on the I/O data bus or to enable buffers to place data on the I/O data bus so that the Microprocessor can read it.

The outputs of U28 are low true pulses of about 500 ns.

Sweep Trigger L

The multiplexer U19 is used to select between LINE or EXTERNAL trigger. When the processor outputs the appropriate bits to the instrument Data Bus (DB 10 thru DB 13) and address 13,B0: (Block K). The output of U18 pins 5 or 7 will select the appropriate U19 input (i.e., U18 pin 7 HIGH selects LINE TRIGGER, U18 pin 5 HIGH selects EXT TRIGGER). U18 Pin 10 is used to disable the RAM Data Unstable Timer (Block E).

The ZON (Z axis on) line is also controlled by U18 in a similar manner. The ZON signal when HIGH will force the Z-AXIS (Block N) to be +5V. U25 is a 3 to 8 decoder which generates 500 nS pulses at its output each time the microprocessor writes to I/O address 13,R1:. By writing appropriate numbers to this register the following events can occur:

* Start the Sweep (U25 Pin 11)

* Stop the Sweep (U25 Pin 12)
* ARM the trigger (U25 Pin 10)
* Clear the BANDCROSS Flip-Flop (Block F) (U25 Pin 15).

U26B Pin 9 is used to stop the sweep, or keep it stopped in the case that it has allready been stopped by a sweep event. The sweep is stopped when the signal is LOW.

Stop Sweep Control M

The sweep can be stopped by any of the following:

1. The BANDCROS signal (LBX) (U12B Pin 5) from the SWEEP EVENT DETECTION (Block F).
2. The BANDCROS signal(LBX) (U12B Pin 5) when driven LOW by the SWEEP GENERATOR board. (NOTE: This will only occure if the MARKER BANDCROSS board fails to stop the sweep before it gets to 12 volts.)
3. The SWEEP TRIGGER (Block L) (U 12B Pin 4) is told to STOP by the processor.
4. The STOP SWP (LSSP) BNC on the rear panel is held low.

The STOP SWP is an IN/OUT signal. As an input signal, LSSP is applied to U12C Pin 9 and is used to generate HSP. As an output signal, it is taken from U13A Pin 1 which is an open collector line pulled up to +5V.

The HSP signal goes to all devices in the instrument that need to respond to the sweep starting and stoping.

CRT Z-Axis Control N

The Z axis signal is normally used to drive the Z axis input of a crt display. When this signal is 0 volts the display will turn its beam on with normal brightness. When it is at +5 volts the display turns its beam OFF (ie. blank). When it is at -5 volts the display intensifies its beam. The 8340A Z-AXIS may be used to turn the display off for bandcrossings, when the sweep is being reset (sweeper retrace, or at other times when the instrument is waiting for a sweep to start. Z-AXIS is also used to show markers by brightening the display. During all other times the Z-AXIS output is at 0 volts.

U21 is a TTL NOR gate. The outputs (U21C and D) are pulled up to +5 Volts in the high state by R37 and R38. U21B is used to provide Op Amp U14 with a low TTL reference voltage. U21D pin 13 is low when either HSP or ZON is high. This output is connected thru R19 to Op Amp U14 which will put 0 Volts on the NEG BLANK output. When both HSP and ZON are low, pin 13 will be HIGH and the NEG Blank output will be at -5 Volts. When U21 pins 10 and 13

are both LOW the Z-AXIS will be 0 Volts. When Pin 10 is HIGH and Pin 13 is LOW Z-AXIS should be -5 Volts. Pins 10 and 13 should never both be HIGH in normal operation. When Pin 10 is LOW and Pin 13 is HIGH Z-AXIS should be +5 Volts. VR1, VR2, and VR3 provide protection against a DC voltage applied to the output connector. C23 and C24 provide frequency compensation to keep the Op amps stable.

Interface Signals:

1. 8410 B INTERFACE: The following signals from this board are needed when the 8340A is connected to the 8410B:

   a. 0 -10v SWEEP (Drives the X axis of the DISPLAY)
   b. STOP SWP (Allows the 8410B/C to stop the SWEEP)
   c. NEG BLANK (Does DISPLAY blanking)
   d. Z-AXIS (Used to generate markers on the DISPLAY)e. 8410 EXT TRIG (Used to initiate 8410B/C to PHASELOCK every time the 8340 PHASELOCKS i.e., new CW frequency or start of sweep.)

2. 8755 C INTERFACE: The following signals from this board are needed when the 8340A is connected to the 8755C and it is desired to use ALTERNATE SWEEP:

   a. 0-10 v SWEEP (DRIVES the X axis on a DISPLAY)
   b. Z-AXIS (Controls Blanking and Marker generation)
   c. LALTEN (Low indicates ALTERNATE mode ENABLED)
   d. LALTSEL (Low indicates ALTERNATE state ACTIVE
   e. LRETRACE (Low indicates RETRACE, used to synchronize with the start of sweep)

3. PLOTTER INTERFACE:

   a. MUTE bar (Used to freeze the servo for BANDCROSSINGS)
   b. PEN LIFT (Used to raise the PEN for RETRACE and, optionally, for bandcrossings)
   c. 0-10v SWEEP (Used to drive the X axis)

A57 MARKER BANDCROSS ASSEMBLY, TROUBLESHOOTING

Troubleshooting of Parts Connected to the Microprocessor Bus

CHECKING MICROPROCESSOR I/O ADDRESS STROBES:

U28 (Block K) is connected to the I/O address buss and generates all of the I/O strobes used on this assembly. The strobes on the output of U28 can be checked using the DSA I/O address test found with the A60 Processor documentation.

An alternate method of checking these signals is to use the front panel and write directly to the I/O addresses while monitering the outputs of U28. This would be done as follows: Push INSTR PRESET, Push the MANUAL sweep key. Connect a Logic probe to the output which is to be checked. Enter into the front panel the corresponding I/O address. The I/O address is written on the lines connected to the output of U28. For example the WRITE RAM signal is marked, 12,R0:. The number 12 is called the CHANNEL and the number 0 is called the SUBCHANNEL. This is entered in the front panel as follows: "SH GZ 12 HZ" - setting the I/O channel and "SH MZ 0 HZ - setting the I/O subchannel. Once this has been done, Push "SH KZ". Make entries by pushing the step keys, using the RPG or by making Data Pad entries. Each entry will cause the WRITE RAM strobe to be generated. This will be a LOW TRUE signal, approximately 500 nS wide, that can be monitered with the logic probe. It can also be seen on a storage scope.

CHECKING MICROPROCESSOR OUTPUT DEVICES:

The following devices are microprocessor output devices: U1, U10, U8, U16, U18, U25, U9, U17 and U23. These can be checked with the DSA I/O data test contained with the A 60 Processor board documentation or can be checked by use of the front panel in a similar maner as above. To do this the I/O channel and subchannel must be entered in the front panel. This can be found by reading the I/O address from the schematic on the write input of the device. After the address has been entered, Push "SH KZ". Entries can now be made directly to the device you are interested in. Monitor the outputs at the same time entering numbers which will affect the signals of interest. For example if the signal of interest is taken from DB2 of the I/O data buss. Enter the number 0 and observe the register output should go LOW, then enter the number 4 and observe that DB2 should go HIGH. Note that if U8 and U16 are being checked, the outputs are only valid during the time the write strobe is LOW. Note that the instrument should be in MANUAL sweep mode so that the normal operation of the instrument dosn't cause the devices being tested to be written to.

CHECKING MICROPROCESSOR INPUT DEVICES:

Input devices can be checked in a similar manner as the output devices. The front panel is used to set up the I/O channel and subchannel as before. U24, U8, and U16 are the only input devices on this assembly. After setting the correct address on the front pannel, Push "SH HZ". Each time "HZ" is pushed the instrument will read from the addressed I/O device and display the results in the entry display in both decimal and octal formats. By shorting each input of the input devices to +5v or ground, each input can be checked.

VERIFICATION

Power On Checks

When the 8340A goes through power ON, the Marker Bandcross Board is partially checked out. The Instrument Controller uses the circuitry in Block A, B, C, and K to verify the I/O data buss. This is done by sending data to the Sweep Event Memory (Block B) and then reading it back. In this maner it can determine if any of the 16 data bits are open or shorted. If the Instrument Check light II, goes off following Instrument Preset, this indicates that the above test has passed.

If the light is ON a problem is indicated. Further information about the problem can be obtained by decoding the 16 self test LEDs on the Processor board. (Refer to the A60 Processor board documentation). When the Marker Bandcross Board is removed from the instrument the front panel Instrument Check light II should go on indicating that this test has failed.

Isolating the Problem

To help verify that the problem is on the A57 MARKER/BANDCROSS Board it may be usefull to remove the A57 assembly and observe the instrument behavior. With A57 removed, the following should occur:

1. Following Power on or Instrument Preset, Instrument Check light II should stay ON and Check light I should go OFF. All 16 self test LEDs on the Processor Board should remain ON.

2. When sweeping, the sweep should stop at 12 volts before resetting. NOTE: the sweep will not be measurable at the front or rear panel connectors since the buffers for these signals are on the A57 board which has been removed. The sweep can be checked on the A58 Sweep Generator.

3. The instrument should lock up properly in CW or MANUAL and perform normally except for the absence of sweep output and display blanking.

4. In a multi band sweep, bandcrossings will all occur when the sweep gets to 12 volts instead of the correct places.

SWEEP DETECTION CIRCUITS: (Blocks A thru F)

Verification (Blocks A - F)

Push the following controls "INST PRESET SWEEP TIME 20 SHIFT SH M2". Observe the left most front panel display. This should

indicate the band number as the instrument goes from band to band. Observe that the green SWEEP LED goes out at band crossings. If the numbers are not changing, this indicatees that LBX (Block F) is not being generated. If the numbers seem to rapidly count from 1 thru 5 , this indicates that LBX (Block F) is not being pulled LOW as it should when the sweep progresses. LBX is the main output of the SWEEP DETECTION circuits.

Troubleshooting (Blocks A - F)

Once deterimined that the problem is in Blocks A thru F, perform the following tests:

Block D.

1. Push the following keys "IP delta F 1MZ SWEEP TIME 10 sec".

2. Verify that U3 pin 16 has a 10 second 0-10V ramp present.

3. Check the B9 thru B0 inputs of DAC U3 for the following:
   B9-1 1 1 1 1 0 1 0 0 0-B0.

4. U3 Pin 15 should be Below 0 volts until the sweep gets to 10 Volts. As the sweep rises above 10 Volts, the voltage at Pin 15 should rise above 0 Volts, and comparior U6 should fire forcing CMP HIGH for about 50 mS.

Block E.

1. Push the following keys "INST PRESET delta F 1 MHz"

2. Trigger a scope on the rising edge of CMP and observe that U5B should have a 700 nS positive pulse at Pin 5 and an inverted identical pulse at Pin 12.

3. Observe that each time U5B files U5A should also fire creating a 5.7 uS positive pulse at Pin 13.

4. Make sure that U5B pin 11 is not stuck low. It should only go low when the 8340A is not sweeping.

Block F

1. Push the following Keys "INST PRESET START FREQ 1 GHz STOP FREQ 13 GHz SWEEP TIME 100 msec M1 8 GHz M2 11 GHz MKR delta "

2. U11B Pin 9 MKR should be a HIGH for 30 mS, then Low for about 100 mS repetively.

3. U11A Pin 5 should go HIGH for about 50 mS when the SWEEP OUT TP5 gets to about 4 Volts, and when the SWEEP OUT gets to 10 Volts there should be another 50mS pulse.

4. U11A Pin 1 should have a single 500 nS pulse applied by U25 at the end of each sweep. If not present check U25 (Block L) using the DSA I/O address bus test found with the A60 Processor documentation.

Block C.

Bi-directional Buffers U8 and U16 are thoroughly verified by the Instrument Preset/Power On test. If Instrument Check Led II is off the Buffers are good. Use the DSA Data Bus Output test to verify data can be sent from DB0-15 to B0-15. To verify the Other direction from B0-B15 to DB0-15 do the following:

1. Press INST PRESET then SINGLE SWEEP. Do a read from address 12,R2: (reads sweep event from RAM). Press SHIFT GHz, enter address 12 and press any terminator (i.e., GHz, MHz, kHz, Hz), press SHIFT MHz, enter sub channel 2, press any terminator, press SHIFT Hz (read).

NOTE

Pressing SHIFT XTAL will cause the 8340A to pause at the next band crossing. Pressing SHIFT Hz may read a different value. Then press SHIFT INT to advance to the next band crossing and SHIFT Hz to read.

2. Observe the entry display should show an octal number and its decimal equivalent. Convert the octal number to binary. This is the number that should be setting on B0 thru B15. It is imortant to realize that in order for B0 thru B15 to be correct, that the SWEEP EVENT MEMORY must have been properly loaded with this number. This loading is done through U8 and U16. It is therefore necessary to first check to see if U8 and U16 can transfer data from the instrument Data Bus to the Marker Bandcross Bus (B0 thru B15). Before Replacing U8 or U16 verify that the two I/O strobes 12,R2: and 12,R0 are being generated by U29 (Block K). If the problem only involves a few bits, the self test leds on the A 60 Processor board can be used to indicate which bits are incorrect. If all leds are on, this indicates that the proplem may have to do with Blocks A B E or K.

Block A

1. Do the following: Press INST PRESET, SINGLE SWEEP, SHIFT XTAL, SHIFT GHz enter 12 and press any terminator, SHIFT MHz, enter 3 and press any terminator, SHIFT KHz (write) enter 0 and press Hz. This should Clear U1 and U10. Verify that lines A0 thru A6 are LOW.

2. Enter the numbers 1,2,4,8,16,32,64 using the front panel. These entries should be latched into U1 and U10 and appear on the A0 thru A6 lines. For example when the number 16 has been entered the A bus should be A6-0 0 1 0 0 0 0-A0.

3. Push "0 HZ SHIFT MHz 0 HZ". The A Bus should be all LOW. Note each time a STEP KEY is pushed the number on the A Buss should be incrememted by 1. The numbers should be 0 = A6-0 0 0 0 0 0 0-A0 32 = A6-0 1 0 0 0 0 0-A0, 15 = A6-0 0 0 1 1 1 1-A0. U29B pin 5 should be HIGH throughout this entire test. Pin 6 should follow Pin 4.

Block B.

Use DSA to check that the READ/WRITE RAM BUFFER (Block C) is able to place data on the B- BUS (B0 thru B 15). Use the Test for Block A to verify the A-BUS can be controlled properly. Verify that U8 and U16 are capable of reading the B-Bus as follows:

1. Press "INST PRESET, SINGLE SWEEP, SHIFT GHz, enter 12 and press any terminator, press SHIFT MHz, enter 2 and press any terminator, press SHIFT Hz (read) SH MZ 2 SH HZ"

2. Alternately short each B-BUS line to + 5V and ground. After each short is made push "SHIFT Hz" note the the octal number in the entry display should indicate the appropriate bit forced HIGH for shorts to +5V and LOW for shorts to ground.

3. If in the above check all pass it should be possible to store and read back numbers in the SWEEP EVENT RAM by doing the following.

   Press:

   INSTR PRESET
   SHIFT XTAL
   SHIFT SINGLE SWEEP
   SHIFT GHz
   1 2 HZ

   Locations in RAM can now be written by pressing:

   SHIFT MHz
   3 Hz

SHIFT kHz (write)
aaa Hz (aaa = RAM address from 0 through 127)

Then press:

SHIFT MHz
0 Hz
SHIFT kHz (write)
ddd Hz (ddd = data to be written to RAM)

It is only necessary to check thru address 15. Use the above to write into RAM a sequece of numbers. Then verify the numbers are properly stored in the RAM by pressing:

SHIFT MHz
3 Hz
SHIFT kHz
aaa Hz
SHIFT MHz
2 Hz
SHIFT Hz

Note: aaa is the RAM address. The read data from the RAM will be displayed in decimal and octal in the entry display. Verify that it matches the sequence of numbers entered.

VERIFICATION AND TROUBLESHOOTING OF BLOCKS G Through N

The Manual Sweep Dac (Block G) and the Sweep Outputs (Block H) can be checked simply by putting the front panel in MANUAL and while monitering the sweep outputs on the front or rear panel turn the RPG and observe that the voltage should be 10 volts when the MANUAL frequency is as high as possible and that it is 0 volts when the frequency is adjusted as low as possible. It should be continuously variable in between. Note: for this test to work the MKR RAMP must be a 0 volts. This should always be the case in MANUAL sweep.

The Sweep Trigger (Block L) can be checked from the front panel. Push "INST PRSET" and observe the green sweep LED. It should be on during the sweep and go out momentarly for each bandcrossing and for the end of sweep. Push the External Trigger button make sure there is no external trigger signal and observe that the sweep stops. Then use a logic pulser or other means to create a single external trigger and verify that the instrument takes a complete sweep but does not continue to sweep. To check the line trigger, lelect delta F and enter 1 MHz so the instrument will be able to make 10 mS sweeps. Observe that the sweep repitition rate is slower when in LINE trigger.

The Sweep Event Dectection circuitry can be verified by making the following set up:

"INST PRESET START 3 GHz STOP 6 GHz M1 4 GHz M2 5 GHz MKR delta 1"

Monitor the Sweep Output and the Z axis signal on a scope. The Sweep Output should stop at 10 volts before being reset for the next sweep. If the sweep goes to 12 volts something is wrong. Observe the Z axis signal to see if the MKR delta is on for the middle portion of the sweep. Now turn off the Delta Marker and observe if two markers are indicated by the Z axis signal. U6 pin 7 should have a pulse on it for each sweep event. If this does not occure, slow down the sweep to 200 Sec and turn all markers off. Measure the inputs of U3 to see if the binary number that is input is correct. It should be 1000 decimal or in binary (bit 10--1 1 1 1 1 0 1 0 0 0--bit 0). This number represents a 10V set point for the comparitor.

The Ram Data Unstable Timer should be checked for the 5.7 uS and 200 nS pulse widths. Make this check by clocking a scope on the CMP signal. The instrument should be in Instrument Preset state.

If U2 and U15 are suspected A0 thru A6 can be checked Via DSA using the I/O data test found with the Processor documentation. If these signatures are incorrect, make sure that the Ram Data Unstable Timmer (Block E) is not clocking the Address Register. This should be disabled by putting the instrument in MANUAL sweep while performing the test.

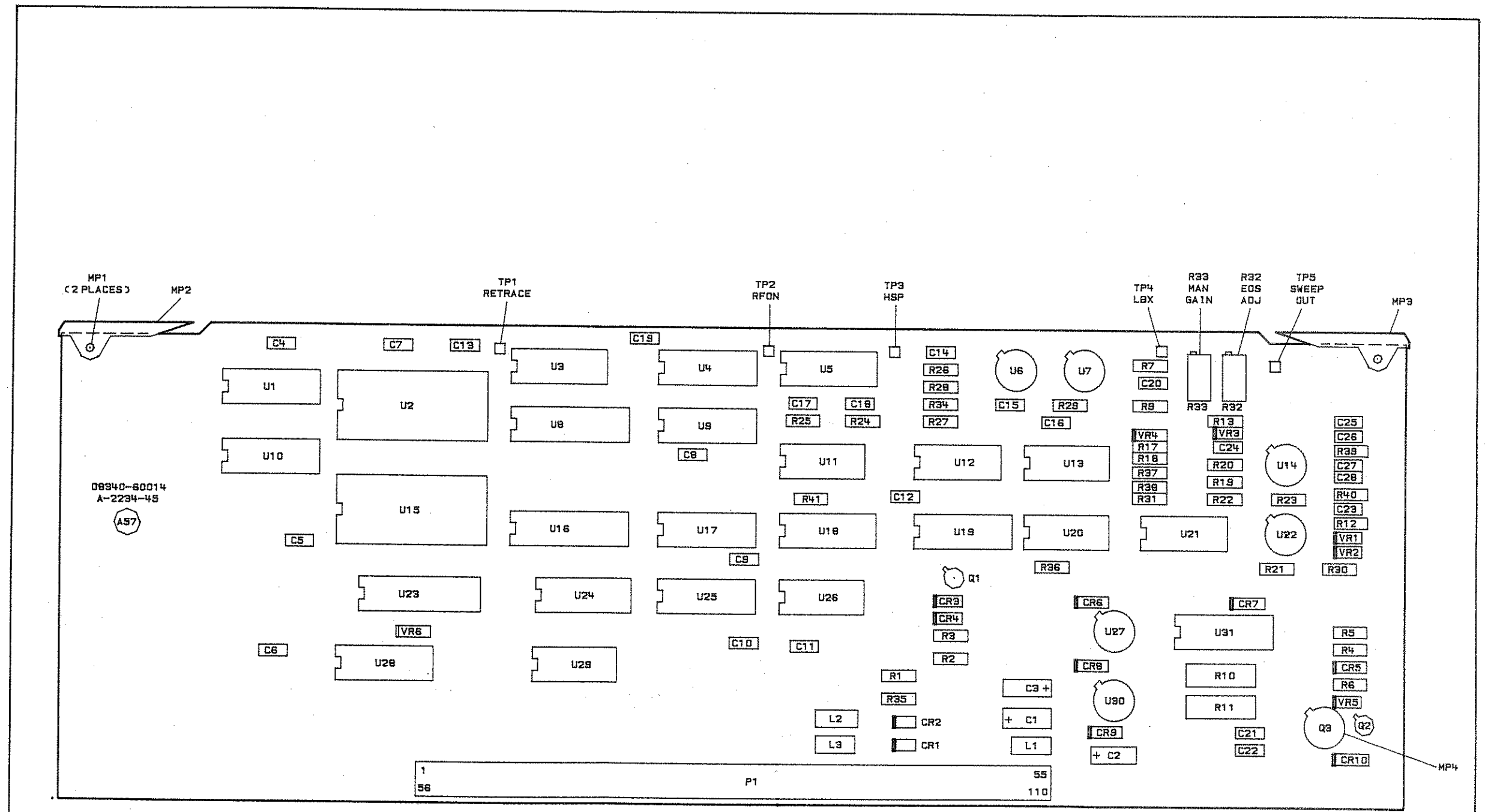
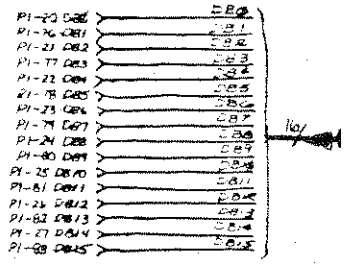
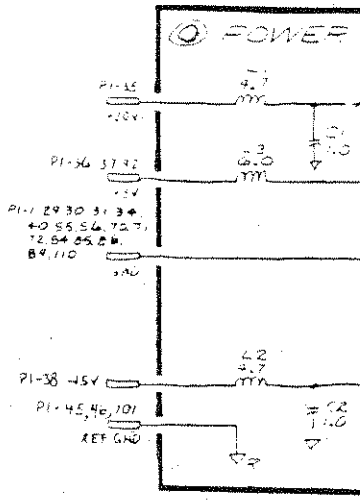


Figure 8-462. A57 Marker/Bandcross,
Component Location Diagram

A57 MARKER/ BANDCROSS 08340-60014





SERIAL PREFIX

SWEEP EVENT DETECTION

(A) ADDRESS REGISTER

U29B U1 +5VF

(B) (12, R0:) (K) (12, R3:)

CTR16 LD [1] LD [2] LD [4] LD [8]

DB6 DB1 DB2 DB3 DB4 DB5 DB6

A0 A1 A2 A3 A4 A5 A6

U10 +5VF CTR16 NC NC NC

(B) SWEEP EVENT MEMORY

+5VF U2 G1

A0 A11 H READ/L WRITE

U15 +5VF G1

RAM B0 B1 B2 B3 B4 B5 B6 B7

RAM B8 B9 B10 B11 B12 B13 B14 B15

(C) READ/WRITE RAM BUFFER

READ (2, R2:) WRITE (K) (12, R0:) (K)

U8 +5VF BUF DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7 B0 B1 B2 B3 B4 B5 B6 B7

U16 +5VF BUF DB8 DB9 DB10 DB11 DB12 DB13 DB14 DB15 B8 B9 B10 B11 B12 B13 B14 B15

(D) SWEEP COMPARATOR

+5VF U3 B0 B1 B2 B3 B4 B5 B6 B7 DAC10 (LSB) (DATA) (MSB) (I OUT) (OFFSET) (FDBK)

R28 100K R26 100K R27 8.25K C13 0.01 C14 0.01 C16 0.01 R29 5.11K C15 0.01 U6 COMP CMP

0V END OF SWP ADJ R32 100 R21 12.1

P1-96(IN) MKR RMP(0-10V)

(E) RAM D… TIMER

CMP +5VF R25 10K C17 810pF

(F) MARKU… FLIP-… U11…

+5V R41 10K U11A

(K) MICROPROCESSOR AND READ WRITE STROBES

U28 +5VF 2.5M 499 1K

P1-15(IN) STOA P1-14(IN) ADR3 P1-9(IN) ADR4

≥ 500nS

P1-17(IN) ADR0 P1-16(IN) ADR1 P1-8(IN) ADR2

15 WRITE RAM (1 RB) READ STB READ RAM (1 RB) WRITE ADDR (1 RB) WRITE STB (1 RB) WRITE CONTROL (1 RB)

P1-13(IN) ENDEC STB

(L) SWEEP TRIGGER

U18 +5VF (13, R0:) R C REG

U19 +5VF

U25 +5VF (3, R1:) CLEAR BAD ADDRESS

U29C 30 IMMEDIATE 2ND IMMEDIATE

U12A +5VF R35 1000 CR1 CR2 R1 1000

P1-9A(IN) LINE TRIGGER

CR3 R3 1000 R2 1000 Q1 CR4

P1-10B(IN) EXT TRIG

U26A +5VF U26B

TRIG ZON

SUPPLIES

+20VF C3 2.2 C4 0.01 C5 0.01 C6 0.01 C7 0.01 C8 0.01 C9 0.01 C10 0.01 C11 0.01 C12 0.01 +5VF

−15VF

(: A-2234-45 DATE: 7-14-82

NOTES

1. REFER TO FIGURE 8-X FOR DETAILED SCHEMATIC DIAGRAM NOTES.
2. RESISTANCE VALUES ARE IN OHMS, CAPACITANCE IN MICROFARADS, AND INDUCTANCE IN MICROHENRIES UNLESS OTHERWISE NOTED.

Figure 8-464. A57 Marker/Bandcross, Schematic Diagram

TP4 TP3 TP5 TP1 TP2

A59 DIGITAL INTERFACE ASSEMBLY, CIRCUIT DESCRIPTION

Introduction

The Digital Interface board communicates to the Micro Processor the tasks which need to be performed. In normal operation of of the instrument, the Microprocessor stops running when all tasks are completed. This control of when the processor runs is done via the (LSTP) control line (Block I). Many I/O addresses are decoded on the board which are used to latch data from the I/O data buss for several assemblies that are external to this board. Some signals are latched on the A59 Digital Interface and then sent to other assemblies via the mother board. An example is Block E.

The HP-IB Interface (Block D) and Phase Lock Indicators and Control (Block B) also reside on the board.

Micro Processor Read/Write Strobes A

The three LS128'S (U12, U19, AND U26) decode 24 possible I/O addresses. The outputs of these 3 to 8 line decoders are used by circuits both on and off the A59 board to clock latches connected to the I/O buss or to Enable Buffers connected to the buss for input operations. There are also several LS 138's on other PC boards where additional addresses are decoded. SIOB is a 500 nS pulse which enables the three LS 138's. While they are enabled the LOGIC signals on ADR0 thru ADR4 are used to select specific I/O addresses. For example, I/O address "3,R3: (Channel 3, Subchannel 3) "causes a 500 nS strobe at (Pin 7 U19) when ADR4-ADR0 are "0 1 1 1 1" and at the same time SIOB is LOW.

Phase Lock Indicators And Control B

The 6 Phaselock Loops in the instrument can be monitored to determine if they are locked by writing into the LS 377 (U24) register a mask that will select idividual LOCK INDICATOR signals and allow the processor to test them via U18 (Block I). During instrument operation, the Instrument Controller will send data to U24 that will set up U25 and U11 to monitor the Phase Lock indicators that should indicate locked for a particular 8340A function. The outputs of U24 Pin 2 and 12 are inverted by U22A and U22B. U22A and B are RS flip-flops wired as inverters. These inverted signals are used to set flip-flops U22C and U22D. The outputs of these flip-flops control the LOCK / ROLL signals for the 20-30 Loop and the YO Loop. Once these flip-flops are set, the the corresponding phaselock loop will try to LOCK UP. This conditon will persist until the set signals are removed and the High Sweep signal (HSP) goes True indicating the Start of a sweep. This will cause the appropriate oscillator to switch from

LOCK to ROLL mode. When the instrument is sweeping, either the YO or the 20/30 oscillator will be allowed to sweep by having its LOCK/ROLL control line set to ROLL. The 20/30 is sweept when the YO Delta F is < 5 mHz. NOTE: The YO Delta F is The Overall sweep width divided by the Harmonic Number (1 thru 4). The remaining outputs of U24 are ANDed with the corresponding Oscillator LOCKED signals and OR ed together by U11 and U25 to generate the UNLOCKED signal.

The DLI (TP4) test point can be pulled to +5volts for trouble shooting to cause the processor to think all oscillators are LOCKED UP when they are not. This should cause the front panel UNLOCKED light to go out.

Change Detector C

Several conditions need to be continously monitored and responded to by the Instrument Controller when they change state. Since the Controller Stops running when it has completed its tasks, this circuit detects changes in instrument conditions and causes the controller to run again so that the changes can be responded to. The Changes that are detected are:

1. OVEN becoming cold or up to temperature.
2. Change in enabled Phase LOCK indicators.
3. Rear panel frequency reference switch set to EXT.
4. LCHNG line being driven low due to one of the following conditions:
   a. Change in the OVERMODULATION indicator.
   b. Change in UNLEVELED indicator.
   c. Service request from the ADC.

When the control signal from the OVEN HOVC falls below 3.5 Volts, the output of comparitor U13 will go HIGH. This Signal is buffered by U7B which drives U6B. U6B will immediately force Pin 4 LOW in responce to the positive going change at Pin 6. When C2 is charged up some 100 uS later, Pin 5 of U6B will go high forcing the exclusive OR gate to return its output to a HIGH. The resulting Negative going pulse from U6B will cause flip-flop U4C to be SET. The output of U4C goes to Block I and causes the Instrument Controller to check for a change in on of the conditions listed above. When the OVEN control signal changes in the opposite direction (i.e., rises above 3.5 volts) U13 will change states again. This change will again cause U6B to create a LOW going pulse about 100 uS wide. Changes in the UNLOCKED and EXternal Reference signals similarly cause LOW going pusles on the LCHNG line. The LCHNG line runs on the A62 Mother Board so that other circuits in the instrument can indicate the need for service from the instrument controller. Where this is done an Exclusive or gate similar to U6B is also used to create LOW going

pulses on LCHNG.

HP-IB Interface D

The HP-IB incorperates the INTEL 8291 HP-IB interface. The additional hardware is to interface it to the Microprocessor. The Physical HP-IB connector and to provide System Controller operation. The LS245 U16 is a Bidirectional Buffer used to interface the 8 bit Data buss DB0-DB7 of U15 to the I/O data buss DT01-DT08. the LS174 U2 latch holds the address of U15 registers that are to be read or written. Also latched in this register are 3 signals which give U15 System Controller operation. This capability is used only for automatic calibration with a Power meter. The 3 signals are:

1. NORMAL/SYSTEM CONTROL - Switches the operation of the HP-IB from normal HP-IB operation to SYSTEM CONTROLLER operation. NOTE: U2 is cleared on POWER ON by the HPUP line. This causes the HP-IB to power up in the NORMAL MODE.

2. ATN - Allows the driving of the ATN signal when in SYSTEM CONTROLLER mode.

3. IFC - Allows the driving of the IFC signal when in SYSTEM CONTROLLER mode. The 6 gates from the U2 take care of the changes that need to be made to convert from NORMAL to CONTROLLER operation. The 75160 U8 and 75161 U14 are the Actual BUSS buffers.

U1A is a buffer with tri state outputs. When it is disabled by a HIGH on pin 1, the signals at its output are not affected in any way. When pin 1 is LOW, Pins 12, and 16 are controlled by U2, Pin 14 is driven HIGH and Pin 18 is driven LOW. U1B is also a buffer with tri state outputs. It is disabled by a LOW in pin 19. Note this is just the opposite of U1A and that both buffers are connected to the same control line. When U1B is disabled, Output pins 7 and 9 are not affected by U1B. When it is enabled, Pin 7 will follow the SRQ signal from U15 pin 27 and Pin 9 will follow the ATN signal from U14. When the HP-IB is in its NORMAL (i.e., non controller) mode of operation, U1A is disabled and U1B is enabled.

M/N Control E

The two LS 174's (U10 and U17) are used by the Instrument Controller to latch control signals necessary to program the M/N Oscillator. This is done when the Instrument Controller does a WRITE to I/O address "3,R3:". The M/N off signal could be used to turn the M/N oscillator OFF. Currently the oscillator is never

turned OFF.

Miscellaneous Inputs F

The LS 244 (U7A) is used to allow the processor to determine if any options are set. Currently None are used. The input on I/O bit 4 (DB4) is tied low and can be used by the processor to determine that the digital interface is present. The processor may choose to ignore the HP-IB if for some reason this BIT is incorrectly HIGH.

Miscellaneous Control G

The LS 377 (U7A) is used by the processor to latch 8 bits of information that are sent to the mother board to control various functions. This is done when the Instrument Controller does a WRITE to I/O address "1,R3:".

HSTD HIGH indicates the internal Frequency Standard has been selected. The Rear panel Switch should cause this signal to change state.

HYGH HIGH increases the GAIN on the YO loop. This is done when the 8340A is in the CW or MANUAL mode.

HFILYO HIGH places a large filter capacitor across the YO coil. This is done in the CW or MANUAL mode.

LRSP LOW causes the Sweep Generator to Reset the Sweep. This is done at the end of every sweep. The RESET signal is removed before the sweep starts.

Timer H

The timer is Started or CLEARED by the Instrument controller and is used to get the controllers attention when the AUTO PEAKING function is turned on. Every 7 minutes the processor will start running and PEAK the RF by optimizing tracking between the YTM and the YO.

U20A is set when the controller does a WRITE to I/O address "2,R0:" and is reset when a WRITE is done to address "2,R1:". When U20A is reset U21 is also reset. When U21A is SET U21 is allowed to start its timming sequence. While U21 is going through its 7 minute count cycle. A 3 second repeating ramp should be seen at pin 7. When the cycle is complete, U20B is SET when U21 pin 3 goes HIGH. The output of U20B goes to Block I where the Instrument Controller is notified that the timmer has completed its cycle. When the controller responds, U20A U21 and U20B will be reset by a WRITE to "2,R1:".

Processor Service Requests I

The LS240 U18 is used by the Instrument Processor to determine which tasks need to be performed. All conditions that need the processor's attention are communicated thru this register except for the front PANEL which can indicate need for service by it's self. All possible reasons for service are ORed by U5 and the result is sent to the processor on the LSRQ line indicating that SERVICE is REQUESTED. The LSTP line is driven by flip-flop U4D which is used to stop the processor from running when all tasks have been completed. U9B in an inverting open collector output buffer. flip-flop U4D is set when the instrument controller does an WRITE to I/O address "5,R0:". This is done to stop the controller when all pending tasks have been completed. U4D is RESET to cause the controller to run again any time LSRQ is driven low. LSRQ can be driven low by U5 thru U3E and U9F or by the Front Panel to indicate a key has been pushed or the RPG has been turned.

The Following Conditions can be monitered when the controller does a READ from I/O address "4,R3:" through U18.

* HP-IB SRQ - The HP-IB interface needs servicing

* BANDCROSS - This line is driven by the LBX (A57 Marker Band Cross Board). After being inverted by U3C, TP6 BC will go high when ever a sweep event occurs. The SWEEP GEN can also drive the LBX line if the sweep ever excedes 13 volts.

* UNLOCKED - An oscillator is UNLOCKED

* EXT. REF.- External Reference is selected by the Rear Panel Frequency Standard INT/EXT Switch.

* OVEN Ready

* POWER FAIL - This indicates that a POWER ON has just occured. This is used by the Processor to determine whether to do a INSTRUMENT PRESET or a POWER ON restore of the LAST STATE. The Processor cannot otherwise distingish between POWER ON and INSTRUMENT PRESET.

* CHANGE FF - One of the Change Detector inputs has changed.

* TIMER- the 7 minute timer has expired.

Power Supply J

The only supply for the board is +5v. L1 and U1 thru C18 provide

required digital filtering.

A59 DIGITAL INTERFACE ASSEMBLY, TROUBLESHOOTING

Troubleshooting Of Circuits Connected To The Microprocessor Bus

Checking Microprocessor I/O Address Strobes (Block A).

U12, U19, and U26 (Block A) are connected to the I/O address buss and generate 24 I/O strobes which are used either on this assembly or are sent via the mother board to other assemblies. These strobes on the outputs of U12, U19, and U26 can be checked using the DSA I/O address test. This test is found with the processor documentation.

An alternate method of checking these signals is to use the front panel to write directly to the I/O addresses while monitering the outputs of one of the LS138 3-to-8 line decoders. This can be done as follows: Push Inst Preset, push the MANUAL sweep key. Connect a Logic probe to the output which is to be checked. Enter into the front panel the corresponding I/O address. The I/O address is shown on the schematic printed above the outputs of the LS138's, in the following form: "m,Rn:" Where m is called the I/O CHANNEL and n is the I/O SUBCHANNEL. For example, assume that we wish to test U19 Pin 7. The I/O address is 3,R3: This is entered into the front panel as follows: "SH GZ 3 HZ", which sets he I/O channel and "SH MZ 3 HZ, which sets the I/O subchannel. Once this has been done, Push "SH KZ", which activates entries to the selected I/O address. Make entries by pushing the step keys, using the RPG or by making Data Pad entries. Each entry will cause the M/N OSCILLATOR CONTROL strobe to be generated. This will be a LOW TRUE signal, approximately 500 nS wide, that can be monitered with the logic probe. It can also be seen on a storage scope. NOTE: I/O address "4,R3:" is dificult to check using the front panel method because the Instrument Controller uses it in the process of operating the front pannel. The "4,R3:" strobe is best checked using the DSA test. The "5,R0:" strobe cannot be checked using DSA because it would cause the processor to go to "SLEEP", it is best checked with the front panel method.

Checking Microprocessor Output Devices (Blocks B, D, E, and G)

The following devices are microprocessor output devices: U24 (Block B) U2 and U16 (Block D), U10 and U17 (Block E) and finally U23 (Block G). These can be checked with the DSA I/O data test contained with the processor documentation or can be checked by use of the front panel in a similar manner as above. To do this the I/O channel and subchannel must be entered in the front panel. This can be found by reading the I/O address on the write input of the device. After the address has been entered, Push "SH

KZ". Entries can now be made directly to the device you are interested in. Monitor the outputs at the same time entering numbers which will affect the signals of interest. For example if the signal of interest is taken from DB2 of the I/O data buss. Enter the number 0 and observe the register output should go LOW, then enter the number 4 and observe that DB2 should go HIGH. Note that if U16 is being checked, the outputs are only valid during the time the write strobe is LOW. Note that the instrument should be in MANUAL sweep mode so that the normal operation of the instrument dosn't cause the devices being tested to be written to.

Checking Microprocessor Input Devices (Blocks D, F, and I)

Input devices can be checked in a similar manner as the output devices. The front panel is used to set up the I/O channel and subchannel as before. U16 and U18 are the only input devices on this assembly. After setting the correct address on the front pannel, Push "SH HZ". Each time "HZ" is pushed the instrument will read from the addressed I/O device and display the results in the entry display in both decimal and octal formats. By shorting each input of the input devices to +5v or ground, each input can be checked. Note that U18 is an inverting buffer so that a LOW at its input should appear as a HIGH at its output.

Change Detectors (Block C)

Connect a logic probe or storage scope to TP8 CHGFF. Observe that a low true pulse is generated each time the rear panel Frequency Standard INT/EXT switch is switched. This should happen for both INT or EXT positions. Also note that the front panel EXT REF LED should go ON when EXT is selected and OFF when INT is selected. The UNLOCKED input can be checked by putting the 8340A into CW and then disconnecting one of the snap on cables which are part of the phase locked loop. This should cause a pulse at TP8 and also cause the Front Panel UNLOCKED LED to go ON. Reconnecting the cable should make it go out. HOVC can be checked by unplugging the 8340A from the AC mains for 5 minutes and then quickly plugging it in and turning it on. The OVEN light should go ON and then after a few minutes the light should go OFF.

HP-IB Interface (Block D)

An 8340A HP-IB operation verification test using an HP 85 desktop computer is provided in Section IV. This test can be used to help troubleshoot HP-IB Interface problems. The program will write to and read from the 8340A. In doing so it checks the handshake lines. The program also checks all data lines and if one or more lines are defective, the program will indicate the defective bits.

The 5mHz Clock signal comes from the Instrument Processor board and is used by U15 to control timming when the 8340A is addressed to talk on the HP-IB buss. The HP-IB will operate normally without this clock if data is only sent to the 8340A.

U1A and U1B can be checked by observing the operation described in the theory of operation. Under all conditions except for the unimplimented auto calibration feature, U1A should be disabled and U1B should be enabled. In this state U1A should have no effect on the surrounding circuits and U1B should mearly connect the SRQ and ATN signals to the HP-IB chip U15.

Timer (Block H)

Verify that the timmer can be reset by pushing the following front panel keys: "IP CW SH GZ 2 HZ SH MZ 1 HZ SH KZ 1 HZ". This should have caused a 500 nS LOW pulse on U20A pin 1. Verify that U21 Pin 6 is LOW and Pin 5 is HIGH. U20B Pin 9 should be LOW. Now verify that the timmer can count by pushing "SH MZ 0 HZ HZ KZ 1 HZ ". This will start the timer. Quickly locate the LSTP test point on the PROCESSOR board and ground it. This will keep the Instrument Controller from servicing the timmer when it completes its 7 minute cycle. Observe 3 second ramps at U21 pin 7. After 128 of these ramps, the output (Pin 3) should go HIGH setting flip-flop U20B. TP1 should go HIGH and stay HIGH. Now remove the ground jumper of the LSTP test point. TP1 should then go LOW.

Processor Service Request (Block I)

U18 can be checked out as indicated in the general trouble shooting of input devices. To check the basic function push the following front panel keys: "IP CW". Note that the RUN light on the PROCESSOR board should be OUT. If it is not, something is pulling down on the LSRQ line or U4D is not being SET by the PROCESSOR as it should. LSTP must be LOW for the PROCESSOR's run light go OUT. NOTE: If the instrument is UNLOCKED due to some hardware problem. The PROCESSOR will RUN continously and LSTP should, in this case, remain HIGH.

Note that by Grounding the LBX test point on the Marker Bandcross Board, that TP6 should go HIGH, LSRQ LOW, LSTP HIGH and by doing a direct READ using the front panel, U18 Bit 14 should appear high in the entry display. This is done by pushing the following sequence: "IP SH GZ 4 HZ SH MZ 3 HZ SH HZ". Note the entry display will have two numbers, the right most will be in the form dddddd. This is an OCTAL (ie. base 8) number. The second digit from the LEFT must be a 4, 6, or 7 in order for BIT 14 to be HIGH.

Isolating A Problem By Removing The Marker/Bandcross Board

To help verify that the problem is on the A57 MARKER/BANDCROSS Board it may be useful to remove the A57 assembly and observe the instrument behavior. With A57 missing, the instrument should do the following:

1. Following Power ON or Instrument Preset, Both Instrument Check lights should go OFF. All 16 self test leds on the Processor Board should go OFF.

2. When the Power is turned OFF and ON the instrument should do a Instrument Preset instead of restoring the prior state.

3. The OVEN annunciator should be ON and the EXT. REF, UNLOCKED, SRQ and REMOTE annunciators should be OFF.

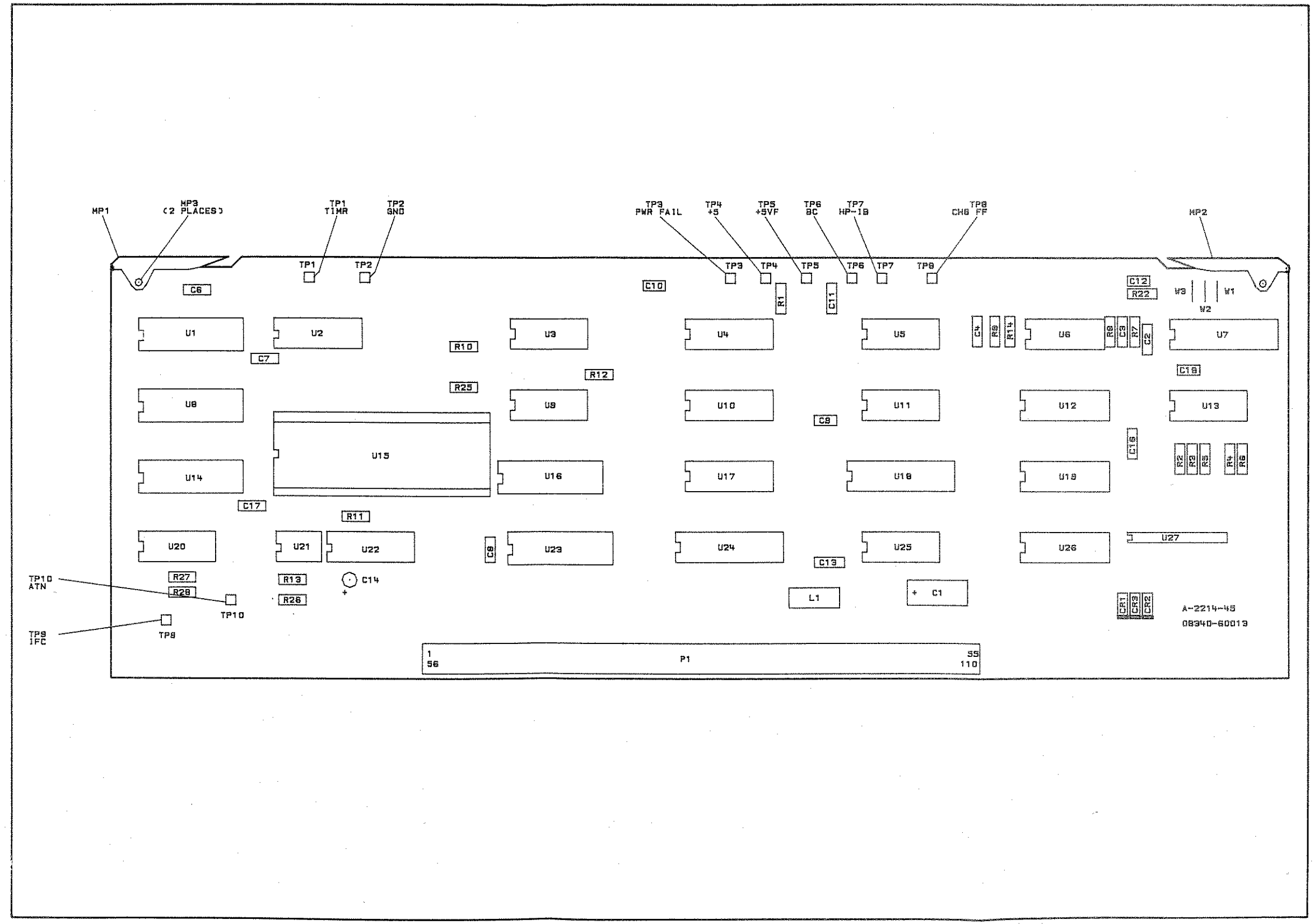
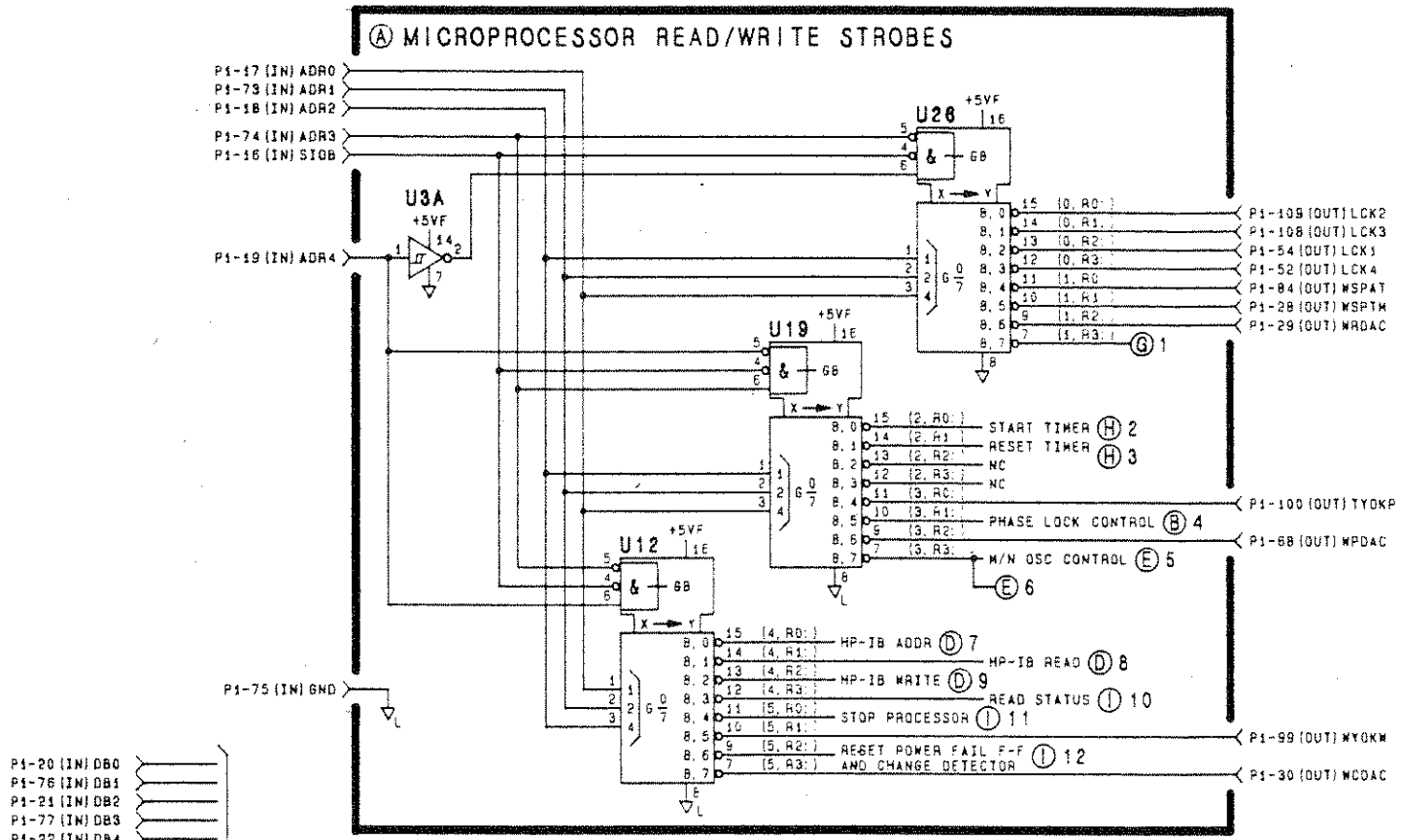
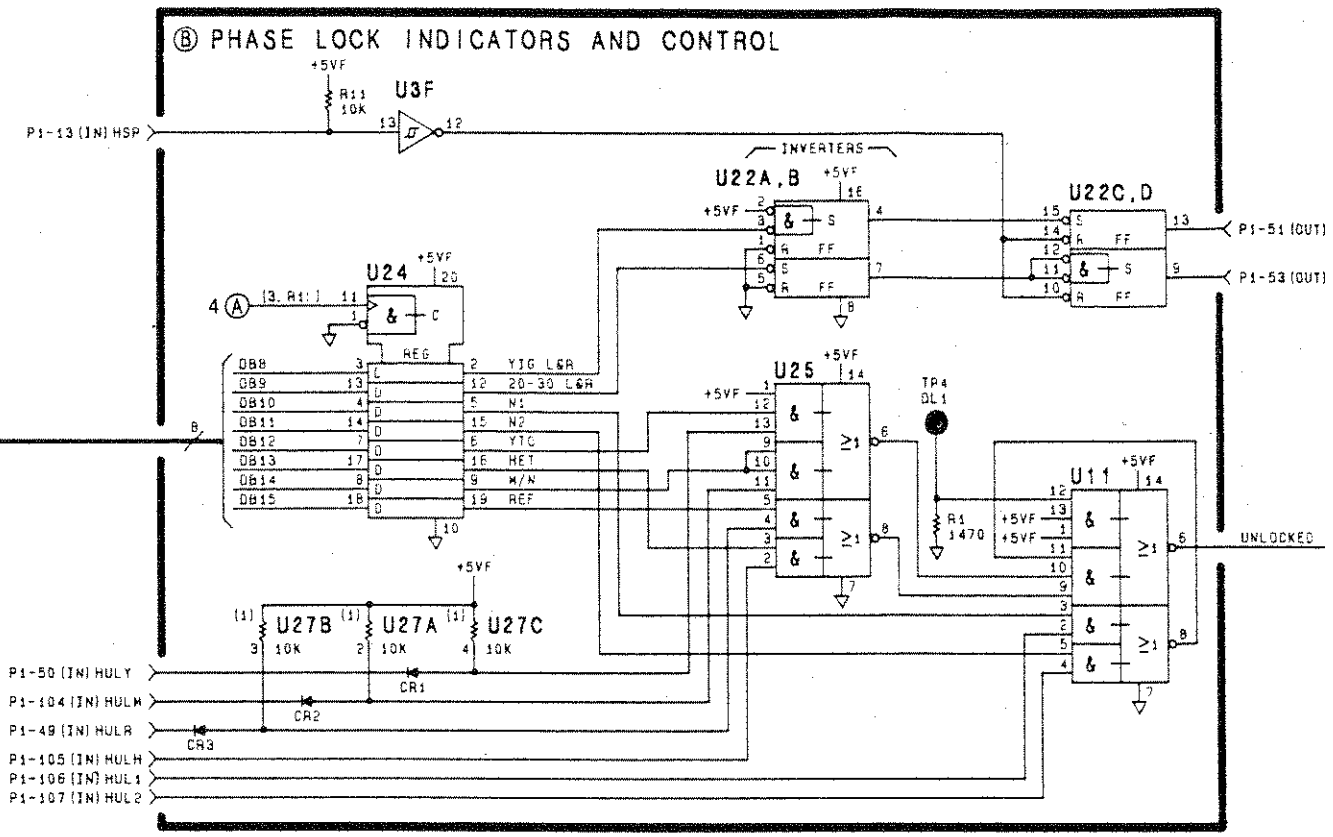
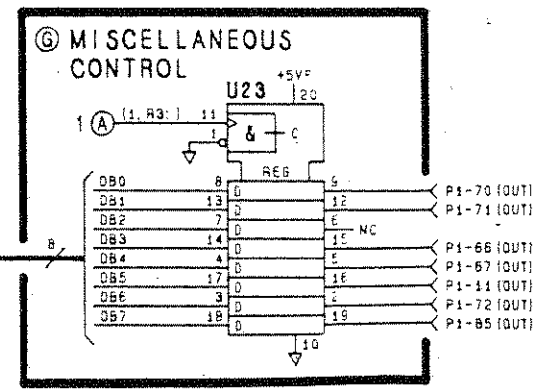


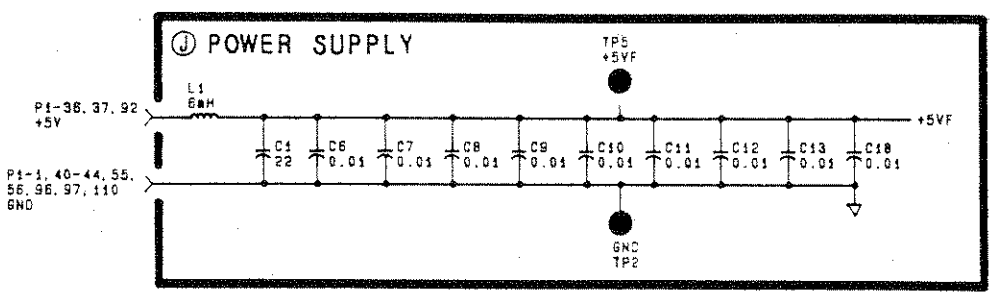
Figure 8-468. A59 Digital Interface, Component Location Diagram

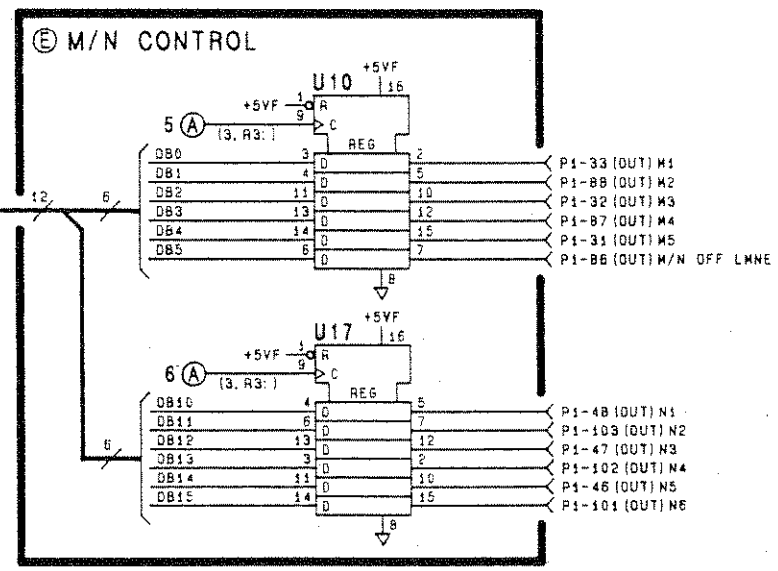
A59 DIGITAL INTERFACE
08340-60013

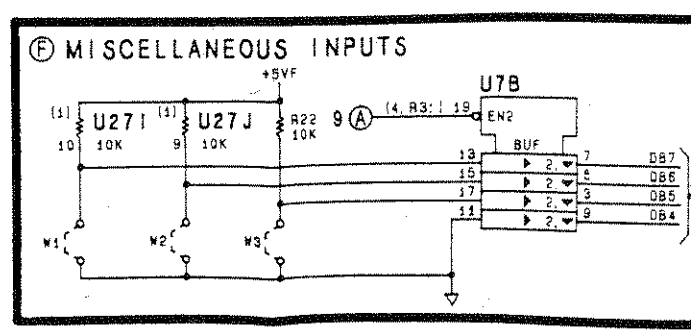












SERIAL PREFIX: A-2214-45 10-25-82 OPII FILE NO. DB4

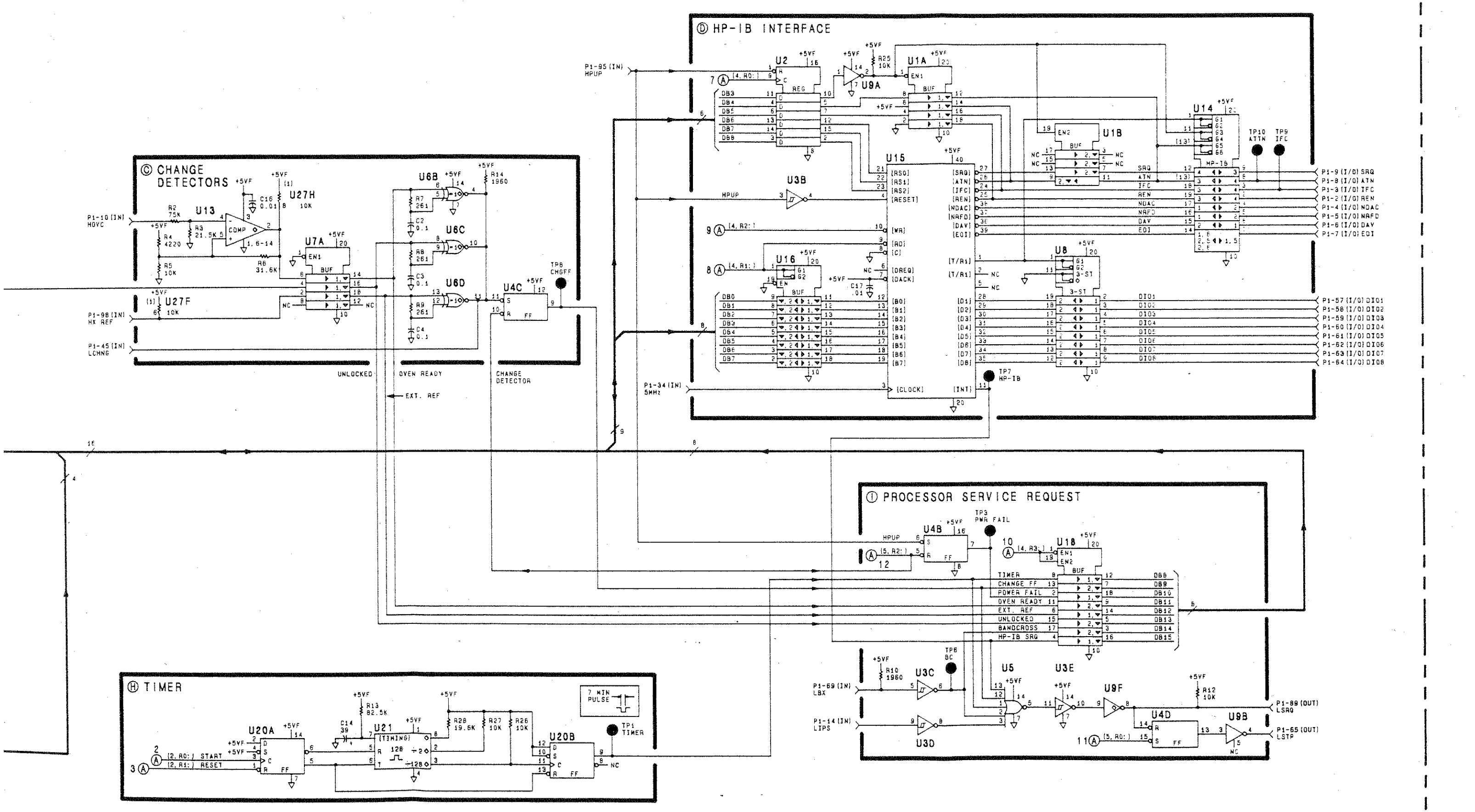


Figure 8-470. A59 Digital Interface, Schematic Diagram

A60 PROCESSOR ASSEMBLY, CIRCUIT DESCRIPTION

The A60 Processor Board contains a 16 bit microprocessor (U7) and is the main instrument controller. The two major interconnections to the Processor Board are to the A61 Memory Board and secondly to the I/O ADDRESS and DATA BUS. There is no memory on the processor Board. The normal sequence of operation is as follows:

1. The processor places an address on the LIDA BUS.

2. The address is latched on the Memory Board by the HSTM signal (Block H).

3. The processor then reads back on the LIDA BUS the instruction or data pointed to by the previously loaded memory address.

4. The processor executes the instruction or processes the data.

5. The execution of an instruction could involve reading data from or writing data to the I/O Address and Data Buses.

6. The sequence begins over again with either the next sequential address and instruction being used or some other address if a jump type instruction was last executed in the processor.

In normal instrument operation the processor stops running when it has nothing to do. This is indicated by the green RUN LED (DS1 Block D) on the Processor Board being turned OFF.

The memory bus or LIDA BUS, is 16 logic signals which carry memory addresses to the A61 Memory Board and also carry data or processor instructions back and forth between the A61 Memory and the A60 Processor boards. The signals in the MEMORY HANDSHAKE block determine how the LIDA bus is used.

Noise Generator A

The frequency of the clock is modulated by the noise generator circuit. This reduces the effect of the continuously running clock on the performance of the 8430A. When the Noise Generator is not working, the 10 MHz clock, will mix with other signals in the instrument and create spurious signals at the output. Diode VR2 is the noise source. Q2 and Q1 amplify the noise signal and diodes CR6 and CR7 limit the signal to 0.5 V Peak to Peak. This noise signal makes small changes to the logic threshold at the input of U1B pin 3.

Clock B

The clock as measured at U12A pin 2 should be 5 Mhz + or - 10%. U1B is connected as a 10 MHz free running oscillator. U12A divides this signal by 2 before it goes to the A59 Digital Interface board and the Clock Driver circuit.

Clock Driver C

The 5 MHz clock is level shifted to 12 volts, shaped and gated to insure non overlaping clocks for the processor.

Stop Processor D

The SYNC line output of U11C is an open collector line used by the processor to HALT or STOP program execution when some internal operation is busy. During Phase 1 of the Clock, the processor always drives SYNC HIGH. When Phase 1 goes LOW one of the internal chips or an external device (U11C) can pull SYNC LOW causing the the processor to WAIT. The processor can be kept IDLE by doing this every time the Phase 1 clock is LOW. This will appear as a 5 mHz signal on the SYNC line. The LSTP line is driven LOW by the A59 Digital Interface Board when all tasks that the processor needs to do, have been completed. This causes the green RUN LED (DS1) to go off and pulses the SYNC line to keep the processor idle. The processor is put in this state to decrease digital noise during measurements.

Pop Synchronizer E

The LIPS (Low Instrument Preset) signal is used to reset the processor and cause the program to start from the beginning. This is done when the front panel INSTRUMENT PRESET button is pushed when the instrument is not in REMOTE. It is also done on POWER ON by the power supply. The flip-flop U12 synchronizes this signal with the processor clock.

SA Timer F

U10 is a 555 timer used to create a 2 to 3 microsecond pulse that is used during trouble shooting to continuously POP the processor. This timer is started by connecting TP1 to +5v and jumpering TP7 timer out to TP6 in Block D.

I/O Address Bus G

All control of the instrument is done by the I/O DATA BUS. Each device on this bus can be distinguished by a unique address. These addresses are generated by the Processor. U16 is an inverting buffer on the I/O address bus. Note ADR5 is never used off the Processor Board. SIOA and SIOB are used by the instrument as strobes to determine when the address lines have valid

addresses on them. SIOB goes LOW for about 1/2 microsecond when a READ or WRITE is to be done using ADDRESS 0 thru 7. SIOA goes LOW for address 8 through 15.

Test Point 4 (LIOSB Block I) goes LOW for all READ or WRITE operations for about 1/2 microsecond. LBUS DIS TP2 (Block G), when grounded will cause all I/O address generation to be ignored.

Memory Handshake H

The instrument's control program and data are stored in the A61 Memory Board. This board communicates with the processor via the 16-bit LIDA (Low Instruction Data Address) Bus and the three control lines: LWRT, HSTM and LSOB.

HSTM (High Start Memory) cycle: While HSTM is low, addresses can be placed on the LIDA lines. On the rising edge of HSTM the address register on the Memory Board is clocked, causing the address to be latched. When HSTM is HIGH the LIDA bus can be used to transmit data or instructions between the processor and the addressed memory location.

LSOB (Low Stay Off Buss): LSOB determines whether the Processor or the Memory Board will drive the LIDA bus. While LSOB is LOW the Memory board is not allowed to drive the LIDA lines. During this time the processor may drive the LIDA bus to send out address or data to memory. U13B functions as an OR gate to cause the Memory Board to get off the LIDA bus if any of the following signals are LOW: HSTM, READ/WRITE, LPDR or RAL.

LPDR (Low Processor DRiving) indicates the processor is sending data on the LIDA bus.

RAL (Register Access Line) indicates the address is that of an internal register.

The LSOB signal is fed back to processor (pin 65) which controls the internal LIDA bus drivers.

LWRT (Low WRiTe). This signal is used to actually cause the writting of data into the RAM on the Memory Board. It is sent TRUE (i.e., LOW) when all three of the following occur:

1. The READ/WRITE line is LOW indicating WRITE.
2. Pin 3 of U2 is Low.
3. Pin 7 of U2 is High.

U2 is a counter used to create a time delay sufficent enough to allow the Memory Board to respond to LIDA bus transfers. The

counter is preloaded to a value of 6 (0110) when HSTM goes HIGH (through U11D and U1C). Except when RAL is HIGH indicating an internal register access. The counter is incremented by the CLOCK. Pins 3 and 7 arrive at the prior mentioned state after 2 counts. This corresponds to the value 8 (1000). U14E is used to feed back to the processor the LUMC signal which indicates the memory cycle is complete.

The normal sequence to fetch and execute an instruction is:

1. The processor places an address on the LIDA BUS.

2. HSTM goes HIGH clocking this address into the Memory Board.

3. LSOB goes HIGH allowing the Memory Board to drive the LIDA bus and preventing the processor from driving the bus.

4. Memory board outputs the addressed instruction and the processor reads it.

5. The processor executes the instruction.

Processor I

The microprocessor is a hybrid circuit built from 3 separate chips. Processor connections fall in 3 major categories: MEMORY Interface(LIDA), I/O Interface(IOB), POWER SUPPLY and CLOCK (U7 Pin 20 and 21).

The remaining connections are:

LINTR (Low Interrupt Request) Pin 1. Requests an interrupt of the processor. This feature is not used in the 8340A and the line should be always high.

LSTS (Low STatuS) Pin 16 (TP13). Is an input to the processor used for self test.

LSRQ (Low Service ReQuest) Pin 17. Is an input to the processor used to indicate to the processor that there is a task for it to perform.

LRAM (Low RAM) Test Point 14 or U7 Pin 15 (Not FLG). Is an input to the processor used in the self test program to call up the destructive RAM test.

SYNC (Pin 29). This signal is used to STOP the processor when all tasks are completed. When the processor is stopped both the LIDA Bus and the I/O Bus are idle. NOTE: When stopped the SYNC has a 5 Mhz signal from the processor on it.

U3 and U5 are octal bidirectional buffers which are used to give the processor sufficent drive capability for the I/O data bus. These are loaded in sockets for trouble shooting purposes.

Self Test J

As part of the self test, the I/O address bus is tested by having the software perform I/O operations to all possible addresses. These addresses are latched into U17 by the IOSB signal. The processor then reads these values back to test them by enabling U17's tristate output onto the I/O DATA BUS. Note that since the upper 8 bits of the DATA BUS (DB8 through DB15) are used to perform this operation, they are tested also.

I/O Data Bus K

The 16 bit I/O DATA BUS (DB0 through DB15) runs throughout the instrument and is the means of communicating with the processor. Data is sent both ways on the bus. U4 and U6 pull the bus up to 5 volts when their is no driver on the bus. This is used mainly for trouble shooting and to allow missing PC boards to be detected by the instrument firmware.

Power Supplies L

Q1 is used to generate the +7VF supply from the +12 supply.

TROUBLESHOOTING

There are four levels of trouble shooting:

1. Self Test. The Self Test is run on power up and after pushing INST PRESET. Two front panel LEDs, CHECK I AND II, give a visual indication of the Self Test results.

2. Signature Analysis. The Signature Analysis Test can be used to verify the results of the Self Test or can be used to do detail troubleshooting of the I/O Address or I/O Data lines.

3. Front Panel or HP-IB Test. The front panel can be used to write to or read from any I/O device.

4. Manual Procedure. The Manual Procedure should be used if the self test does not run. Observe the 16 A61 LED indicators. At power up or INST PRESET all 16 LEDs should turn ON for about 1 second. During the next 2 seconds some of the LEDs should go OFF and ON again. If this happens the self test is running. If all 16 LEDs go ON and remain ON the self test is not executing.

I. SELF TEST

A. DESCRIPTION

The Self Test is run on power up and after pushing INST PRESET. Two front panel LEDs, CHECK I and II, give a visual indication of the self test results. The Self Test automaticly performs the following tests:

1. PROCESSOR TEST - Computations are done in the internal microprocessor registers and compared with a check sum stored in ROM.

2. RAM TEST

   a. With TP 14 NOT grounded. About 1/2 of the locations of RAM are read, complemented, rewritten, complemented, and then finally restored to original value. Note this check will not catch RAM addressing problems.

   b. With TP 14 grounded. All RAM is sequentialy exercised by writing the address in each location and then repeating the test with complemented addresses.

CAUTION

This will cause any stored calibration data or SAVE registers to be lost.
NOTE: On MEMORY Boards built since 1983 an additional test point on the MEMORY Board will need to be grounded to enable the Protected Portion of RAM to be exercised. If all of memory cannot be exercized the test will indicate failure.

3. ROM TEST - Each ROM location is summed. The sum for each ROM is compared with checksums stored in ROM.

4. I/O ADDRESSING TEST - All addresses are set up and then read back into the processor. The sum of the results is compared with a checksum stored in ROM. If this test passes the upper 8 bits of the DATA BUS can also be considered good.

5. I/O DATA TEST - The 16 bit DATA BUSS is exercised by using the hardware on the Marker Bandcross Board to read and write to the I/O BUS.

NOTE

By grounding TEST POINT 1 (LSTS) the Self Test will be continously executed.

B. FRONT PANEL INSTRUMENT CHECK LEDS I and II

1. The instrument power supply comming up should cause both LEDs to be turned on.

2. LED I will be turned OFF when it is determined that all ROM, RAM, and the LADR bus are good and that the microprocessor works.

3. LED II will be turned OFF when it is determined that the I/O ADDRESS BUS and all 16 bits of the I\O DATA BUS are good.

4. If either LED stays on further isolation of the problem can be made by examining the 16 LEDs on the A61 Memory Board. When all 16 A61 LEDs are OFF, front-panel LED II should be OFF.

5. It is possible that a fault can occur which will cause the CHECK LEDs to go out when they shouldn't. If this happens the LEDs on the Memory board will verify this condition (i.e., One or more A61 LEDs will be on).

C. SELF TEST LEDS ON MEMORY BOARD (fault LEDs)

1. When the Self Test finds no fault conditions the LEDs should go OFF about 1 second after power ON, or after INST PRESET, and then stay OFF.

2. When the Self Test finds a fault condition it is displayed as follows: When power is turned on all LEDs are turned on for about 1 second. After this The LEDs display ROM, RAM, processor and I/O addressing status for 2 seconds. Afterwards the LEDs display I/O DATA BUS errors. If the difficulty involves the I/O ADDRESS or I/O DATA BUS; it will be helpfull to selectively remove PC boards that interface to the I/O bus until the problem is cleared. The only PC boards, other than power supply boards, that must be in the instrument to make the Self Test operate, are the A60 Processor, the A61 Memory and the A57 Marker Band Cross Board. The I/O address test is valid even with the Marker Band Cross Board missing. If the I/O address test passes it is also indicates that data bits 8 through 15 are good. Refer to table at end of the Self Test description to learn which assemblies interconnect to the digital buss.

3. If all 16 LEDs stay lit for the entire time, it will be necessary to resort to manual troubleshooting of controller hardware.

LED	1st SECOND:	next 2 SECONDS	afterward
LED 15	light on	light out	I/O Bit 15 FAIL
LED 14	light on	I/O DATA TEST FAILED	I/O Bit 14 FAIL
LED 13	light on	I/O ADDRESS TEST FAILED	I/O Bit 13 FAIL
LED 12	light on	*RAM U20 TEST FAILED	I/O Bit 12 FAIL
LED 11	light on	*RAM U20 TEST FAILED	I/O Bit 11 FAIL
LED 10	light on	*RAM U5 TEST FAILED	I/O Bit 10 FAIL
LED 9	light on	*RAM U5 TEST FAILED	I/O Bit 9 FAIL
LED 8	light on	ROM U9	I/O Bit 8 FAIL
LED 7	light on	ROM U24	I/O Bit 7 FAIL
LED 6	light on	ROM U8	I/O Bit 6 FAIL
LED 5	light on	ROM U23	I/O Bit 5 FAIL
LED 4	light on	ROM U7	I/O Bit 4 FAIL
LED 3	light on	ROM U22	I/O Bit 3 FAIL
LED 2	light on	ROM U6	I/O Bit 2 FAIL
LED 1	light on	ROM U21	I/O Bit 1 FAIL
LED 0	light on	PROCESSOR TEST FAILED	I/O Bit 0 FAIL

* Ram Test is not exhaustive unless TEST POINT 14 is grounded

CAUTION

This will cause any stored stored calibration data or SAVE registers to be lost.

II. SIGNATURE ANALYSIS TEST

The Signature Analyzer can be used to verify the results of the Self Test or can be used to do detail troubleshooting of the I/O Address or I/O Data lines.

Four test points are provided on the A61 Memory Board to start or stop the GATE of the Signature Analyzer. The rising edge of the signal on these test points is to be used. A61 TP9, 8, 7, 6

T3	T2	T1	T0	
0	0	0	0	
0	0	0	1	Beginning of Self Test
0	0	1	1	End of Self Test, Begin OUTPUT EXCERISE
0	1	1	1	End of OUTPUT, Begin INPUT EXCERISE
1	1	1	1	End of INPUT EXCERIZE

A. Signature Analyzer Self Test Verification.

Connect Signature Analyzer as follows:

GND to ground Connect Probe to +5 volts
CLOCK to HSTM
START to T0
STOP to T1

This test provides an alternate method of reading out the results of the SELF TEST LEDs. The easier way is to observe the red LEDs on the MEMORY board.

Possible signatures:

399F	Test Passed
3494	LED 0 On
FH25	LED 1 On
C349	LED 2 On
AFH2	LED 3 On
2C34	LED 4 On
8AFH	LED 5 On
A2C3	LED 6 On
A8AF	LED 7 On
2A2C	LED 8 On
FA8A	LED 9 On
72A2	LED 10 On
9FA8	LED 11 On
672A	LED 12 On
99FA	LED 13 On
P672	LED 14 On

B. OUTPUT EXERCISE

This test will cause a fixed pattern to be output on the I/O DATA BUS (DB0 through DB15) and the ADDRESS BUS which will cause
data to be sent to all addresses on the bus except for the Attenuator, the Go to Sleep Flip Flop, and all addresses assigned as input devices.

To perform test:
1. Ground A60 TP13 TP LSTS (Block H)
2. Turn power OFF and ON.
3. Connect Signature Analyzer as follows:

   START - A61 TP7 T1 (Block C) rising edge
   STOP - A61 TP8 T2 (Block C) rising edge
   CLOCK - A60 TP4 LIOSB (Block H) rising edge
   GROUND - chassis

   NOTE: +5V signature to be 2019.

4. The following signatures are to be found on the I/O DATA and ADDRESS BUS as measured on any point along the bus.

   For example A60

	PIN on A60P1	Mnemonic	SIGNATURE
	15	SIOA	1714
	16	SIOB	370H
	19	ADR4	7UUF
	74	ADR3	8U24
	18	ADR2	012F
	73	ADR1	U154
	17	ADR0	AUCU
*	83	DB15	H186
*	27	DB14	CF15
*	82	DB13	37FH
*	25	DB12	3H44
*	81	DB11	9PA2
*	25	DB10	FU51
*	80	DB9	67A8
*	24	DB8	P702
*	79	DB7	2757
*	23	DB6	F77H
*	78	DB5	63CP
*	22	DB4	CC29
*	77	DB3	0942
*	21	DB2	H077
*	76	DB1	CFPH
*	20	DB0	0AA0

   * Signals indicated by a star, should have the same signatures on both sides of the

bidirectional buss buffers on the Processor Board. These IC's are on sockects so they can be used to isolate faults between the Processor Board and the rest of the instrument.

5. The following signatures are the I/O ADDRESS BUS signatures as measured on pins of the microporcessor. The signals are inverted by a buffer before going off the board.

U7 Pin	Mnemonic	SIGNATURE
7	LADR0	8UA6
6	LADR1	H14H
80	LADR2	2135
79	LADR3	AU3H
78	LADR4	5UP5
77	LADR5	1714

6. By having previously recorded the signatures that should exist on boards that take data from the I/O BUS (following table), it is possible to troubleshoot by comparing the signatures from the instrument under test to the known good signatures.

NOTE

By grounding A60 TP2 LBUS DISABLE, bus drivers that are being incorrectly enabled onto the bus due to an addressing error can be disabled.

Following is a complete list of the signatures of latched data bits for the various addresses throughout the instrument. These signatures can be measured by probing the output side of noninverting latches located on the data bus in various parts of the instrument.

ADDRESS		DATA BIT											
		0	1	2	3	4	5	6	7	8	9	10	11
CH	SUB									12	13	14	15
0	0	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx
										xxxx	xxxx	xxxx	xxxx
0	1	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx
										xxxx	xxxx	xxxx	xxxx
0	2	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx
										xxxx	xxxx	xxxx	xxxx
0	3	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx
										xxxx	xxxx	xxxx	xxxx
1	0	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx
										xxxx	xxxx	xxxx	xxxx
1	1	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx
										xxxx	xxxx	xxxx	xxxx
1	2	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx
										xxxx	xxxx	xxxx	xxxx
1	3	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx
										xxxx	xxxx	xxxx	xxxx
2	0	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx
										xxxx	xxxx	xxxx	xxxx
2	1	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx
										xxxx	xxxx	xxxx	xxxx
2	2	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx
										xxxx	xxxx	xxxx	xxxx
2	3	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx
										xxxx	xxxx	xxxx	xxxx
3	0	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx
3	1	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx
										xxxx	xxxx	xxxx	xxxx
3	2	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx
										xxxx	xxxx	xxxx	xxxx
3	3	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx
										xxxx	xxxx	xxxx	xxxx
4	0	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx
										xxxx	xxxx	xxxx	xxxx
4	1	This address is an input device.											
										xxxx	xxxx	xxxx	xxxx
4	2	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx
										xxxx	xxxx	xxxx	xxxx
4	3	This address is an input device.											
5	0	This address is the GO to SLEEP flip flop.											
5	1	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx
										xxxx	xxxx	xxxx	xxxx
5	2	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx
										xxxx	xxxx	xxxx	xxxx
5	3	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx	xxxx
										xxxx	xxxx	xxxx	xxxx

```
 6  0 CC23 0UFP 6614 C5A1 12FC 10PH H7A5 20CH 38U3 086U P6A0 FH41
                                              9A82 CAU3 0F6P 6155
 6  1 8H01 2156 79U9 F8A6 AA19 H973 AP4U 7C63 FH92 A070 5F49 C892
                                              7124 5FC5 C03U 5C2A
 6  2 xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx
                                              xxxx xxxx xxxx xxxx
 6  3 This address is an input device.

 7  0 xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx
                                              xxxx xxxx xxxx xxxx
 7  1 xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx
                                              xxxx xxxx xxxx xxxx
 7  2 xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx
                                              xxxx xxxx xxxx xxxx
 7  3 This address is an input device.

 8  0 xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx
                                              xxxx xxxx xxxx xxxx
 8  1 xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx
                                              xxxx xxxx xxxx xxxx
 8  2 xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx
                                              xxxx xxxx xxxx xxxx
 8  3 xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx
                                              xxxx xxxx xxxx xxxx
 9  0 xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx
                                              xxxx xxxx xxxx xxxx
 9  1 xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx
                                              xxxx xxxx xxxx xxxx
 9  2 xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx
                                              xxxx xxxx xxxx xxxx
 9  3 xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx
                                              xxxx xxxx xxxx xxxx
10  0 xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx
                                              xxxx xxxx xxxx xxxx
10  1 xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx
                                              xxxx xxxx xxxx xxxx
10  2 F263 A37H 6140 P53C PHFH 2U1H 24UF 1484 0PC3 3AHF 0U7P xxxx
                                              xxxx xxxx xxxx xxxx
10  3 This address is an input device.

11  0 xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx
                                              xxxx xxxx xxxx xxxx
11  1 xxxx xxxx xxxx 2U45 H706 60C7 8U2H H995 3AA6 UFF0 C7F2 xxxx
                                              xxxx xxxx xxxx xxxx
11  2 xxxx xxxx xxxx 9A42 U1C7 8A0F 2623 CC4U C3AF A26A 76PU xxxx
                                              xxxx xxxx xxxx xxxx
11  3 xxxx xxxx xxxx A4A5 4484 222P xxxx xxxx xxxx xxxx xxxx xxxx
                                              xxxx xxxx xxxx xxxx
```

```
12  0 xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx
                                                xxxx xxxx xxxx xxxx
12  1 This address is an input device.

12  2 This address is an input device.

12  3 xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx
                                                xxxx xxxx xxxx xxxx
13  0 xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx
                                                xxxx xxxx xxxx xxxx
13  1 xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx
                                                xxxx xxxx xxxx xxxx
13  2 xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx
                                                xxxx xxxx xxxx xxxx
13  3 xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx
                                                xxxx xxxx xxxx xxxx
14  0 xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx
                                                xxxx xxxx xxxx xxxx
14  1 xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx
                                                xxxx xxxx xxxx xxxx
14  2 xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx
                                                xxxx xxxx xxxx xxxx
14  3 xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx
                                                xxxx xxxx xxxx xxxx
15  0 A18U 9A09 PH05 031F HU2P 508P xxxx xxxx xxxx xxxx H05A A0C4
                                                4169 15HH U2AH 3F4F
15  1 xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx xxxx
                                                xxxx xxxx xxxx xxxx
15  2 5056 A239 46P7 8U5C 1F22 73C7 P76U FF4C xxxx xxxx xxxx xxxx
                                                xxxx xxxx xxxx xxxx
15  3 This address is an input device.
```

C. ADDRESSING EXERCISE - (OUTPUT EXCERISE and INPUT EXCERISE)

This test does the same outputting of data as in the previous test. In addition all the Input devices are read from. This combined test makes it possible to troubleshoot problems on the I/O ADDRESS BUS or address decoding on any board in the instrument.

1. Ground A60 TP 13 STS (Block H)
2. Turn power OFF and then ON
3. Connect Signature Analyzer as follows:

```
START - A61 TP7 T1              rising edge
STOP  - A61 TP9 T3              rising edge
CLOCK - A60 TP4 LIOSB           rising edge
GROUND - chassis
CHECK + 5V signature = FU0A
```

Measure signatures as follows:

MNEMONIC	A60 P1	SIGNATURE	U16-U20	SIGNATURE
SIOA	Pin 15	A1F0	U20 Pin 12	xxxx
SIOB	Pin 16	6PFA	U20 Pin 14	xxxx
ADR4	Pin 19	P3H8	U16 Pin 12	xxxx
ADR3	Pin 74	234U	U16 Pin 14	xxxx
ADR2	Pin 18	66F3	U16 Pin 2	xxxx
ADR1	Pin 73	A1F4	U16 Pin 4	xxxx
ADR0	Pin 17	UP5C	U16 Pin 6	xxxx

Signatures for U15:

MNEMONIC	U15	SIGNATURE
LAD0	Pin 1	3151
LAD1	Pin 2	6PFP
LAD2	Pin 3	A9F9
LAD3	Pin 4	PF45
LAD4	Pin 5	2FH2
L SIOB	Pin 6	A1F0
Ch 7: Sub Ch 3	Pin 15	FU2A

Following is the list of signatures that corresponds to all decoded I/O strobes. These are usually generated by an LS 138 connected to the I/O address buss.

I/O ADDRESS Channel, SubChannel		STROBE SIGNATURE
0	0	2P0H
0	1	234C
0	2	F4A0
0	3	3H6A
1	0	4PS6
1	1	10F1
1	2	3169
1	3	7P86
2	0	03FA
2	1	2FF7
2	2	9189
2	3	4844
3	0	532A
3	1	FSA9
3	2	94C8
3	3	C34A

4	0	P06F
4	1	FP08
4	2	CCAC
4	3	FU8C
5	0	go to sleep flip flop
5	1	UC91
5	2	8389
5	3	PFHH
6	0	A3U2
6	1	7311
6	2	C403
6	3	FU4A
7	0	28UF
7	1	SCF2
7	2	1SC0
7	3	FU2A
8	0	H6H3
8	1	94A7
8	2	FPAH
8	3	AC21
9	0	U17P
9	1	A6H2
9	2	8740
9	3	12AC
10	0	3FPA
10	1	9H7C
10	2	H43P
10	3	FU1A
11	0	9163
11	1	C8F2
11	2	0FC3
11	3	U48U
12	0	U073
12	1	FU02

12	2	FUOP
12	3	2PFC
13	0	CUFA
13	1	U930
13	2	U8A4
13	3	8H6U
14	0	9A5U
14	1	4HCA
14	2	UU41
14	3	3136
15	0	1UH5
15	1	11PO
15	2	H577
15	3	FUO8

III. FRONT PANEL or HP-IB DIGITAL TROUBLE SHOOTING

Any I/O device can be writen to or read from by use of the front panel. This capability is used through shift functions that are on the four numeric terminator keys (SHGZ, SHMZ, SHKZ, SHHZ).

SHIFT GHz - allows the I/O channel to be set up, (0 thru 15).

SHIFT mHz - allows the I/O subchannel to be set up (0 thru 3).

All I/O addreses are made from a Channel and a Sub Channel number. These numbers should be available from schematics for boards which interface to the I/O buss.

SHIFT kHz - will cause subsequent numeric entries to be written directly to the address set up in channel and subchannel.

SHIFT Hz - causes the set up address to be read from and the results displayed in the entry display.

A. INPUT REGISTER TEST

Set up the CHANNEL and SUBCHANNEL as indicated above for the input device that is to be tested. Locate the physical device and one by one short each input to +5volts and then Ground. By pushing Shift, Hz each time a pin is shorted the results will be displayed in the ENTRY display. The displayed number will be in both OCTAL and DECIMAL. Observe in the OCTAL display that the appropriate bits go HIGH or LOW

as would be caused by shorting the inputs HIGH or LOW.

B. OUTPUT REGISTER TEST

Set up the CHANNEL and SUBCHANNEL as described above for the output device that is to be tested. Use a Logic Probe to examine the outputs of the device and write directly to the device by pushing shift Khz and then making entries. For example Enter 0 then -1 this should make the latched output of all bits go low and then High.

NOTE

Many address are written by the instrument firmware as the instrument goes thru its phaselock operation. This could cause information that is written from the front panel to be overridden. One way to avoid this is to put the instrument into MANUAL such that it is not sweeping. There are some addresses, like the front panel LEDs that will be over written by the firmware regardless.

IV. MANUAL TESTS

The following MANUAL procedure should be followed if the A61 Self Test Indicator LED FAULT register has all LEDs lit for the entire time following power on.

The objective of the MANUAL tests is to get the Self Test operational as quickly as possible.

A. Check all Power supplies On (A60 Processor and A61 Memory Board.

B. Check green RUN LED on the Processor Board. If not ON remove the A59 Digital Interface which is the only board that can STOP the processor.

C. Check the LIPS (A60TP6 Block D) to make sure the instrument isn't continuously being PRESET. If this line is LOW check if the power supply is incorrectly driving the line.

D. Check the CLOCK signal on the processor. 12 Volt 5 mhZ signals should be present on microprocessor pins 20 and 21.

E. Perform FREE RUNNING POP test

1. The Free-Running POP test checks the LIDA Bus, the A61 MAR Bus, and the A61 ROM. The A60 SA Timer (Block E) output (TP7) is connected to LIPS (A60TP6 POP Synchronizer Block D). This continually resets the processor to a known state: it continually executes the first instruction (at location 40) which in turn reads all the rest of ROM memory.

   a. Jumper A60TP1 (TIMMER ON) to A60TP11 (+5V).

   b. Jumper A60TP7 (TIMER OUT) to A60TP6 (LIPS).

   c. Externally trigger oscilloscope off the falling edge of A60TP5 (POP OUT).

   d. Monitor A61TP1 (HSTM) on one channel of an oscilloscope.

   At the rising edge of the 2nd HSTM pulse 1.25 us microsecond pulses should be present on the MAR lines. Except for MAR5, all pulses will be positive going transitions.

   If the appropriate pulses are present on the MAR lines use an oscilloscope and check the waveforems as shown in Figure * . Memory Timing.

2. Refer to Figure * . A60 Processor Timing and Figure * . Memory Timing and check for the waveforms as shown. Also check the 5 MHz two phase clock waveform as shown in Figure * . The following is the sequence that generates these waveforms:

   a. POP input to the processor goes high (Start of sequence).

   b. Processor outputs the starting address (Octal 40) onto the LIDA Bus. The processor also sets LREAD/WRITE HIGH (write) and RAL (Internal Register Address) HIGH.

   c. Processor forces HSTM (Block G) HIGH, clocking the address from the LIDA Bus into the MAR (Memory Address Register) on the A61 Memory Board.

   d. LSOB goes HIGH when the processor sets LREAD/WRITE LOW indicating that the processor no longer drives the LIDA Bus. When LSOB is HIGH, the memory board is allowed to drive the LIDA Bus and thus memory data appears on the LIDA Bus.

   e. When timer A60 U2 times out, U14E output (LUMC) is fed

*To be supplied.

back to the processor to indicate that the memory cycle is complete.

f. The processor reads the instruction and forces HSTM LOW which also forces LSOB LOW.

g. To execute the first instruction, steps (b) through (f) are repeated, only the address output is an indexed address that is continually decremented so all possible addresses are exercised.

At the rising edge of the 2nd HSTM, address information should be on the LIDA lines with appropriate HIGH and LOW levels.

At the falling edge of the 2nd HSTM, memory data is on the LIDA lines. They should show good HIGH and LOW logic levels and may show some open, intermediate states.

h. At the 3rd HSTM, no LSOB is generated since it is an internal address. RAL line goes HIGH keeping LSOB LOW.

i. During a write operation (5th HSTM), LSOB is LOW and a 200 nanosecond LWRT pulse is generated. The processor outputs data onto the LIDA Bus which is written into the A61 RAMs.

Suggestions* After connecting the jumpers, check the HSTM (A61TP1) and LSOB (A61TP2) lines for activity. If they appear good, go ahead and check the LIDA lines when the indexed address and data are on the bus at the 2nd HSTM as described in step (g). If HSTM or LSOB is bad, then begin with step (a) and verify each step.

To help isolate a stuck LIDA line:

Grounding LSOB (A61TP2) should force all drivers on the A61 board into the high impedance third state.

Check all A60-U7 microprocessor 16 LIDA lines and pins 29, 25, 65, 82, 34, 30, 31.

NOTE: The short pop test verfies the processors ability to address all memory and execute one instruction. (i.e., WBD inst= withdraw byte from memory). For the processor to read this one instruction out of the first pair of ROMS, control signals Vpp and EN must be at zero volts. This should cause the ROM to output data on the LIDA bus.

DIGITAL BUS INTERCONNECTION QUIDE

R = receiver, D = driver, B = both

ASSEMBLY DESIGNATOR	I/O DATA BUSS DB 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	I/O SI O A	SI O B	ADRS BUSS 4	3	2	1	0
PS A19																							
PS A35																							
PS A52																							
PS A53																							
PS A56																							
PS A62																							
FP A1																							
FP A2																							
FP A3	R	R	R	R	R	R			R	R	R	R	R	R	R	R							
FP A4																							
FP A5																							
FP A6	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B		R	R	R	R	R	R
FP A7																							
MC A57																							
MC A58	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
MC A60	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B		R	R	R	R	R	R
FC A54				R	R	R	R	R	R	R	R	R	R	R	R								
FC A55																							
FC A59		R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		R	R	R	R	R	R
FC A61	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	R		R	R	R	R	R
YO A22																							
YO A48																							
YO A49																							
YO A50																							
FM A23						R	R	R			R												
ALC A21																							
ALC A24			R	R	R	R	R																
ALC A25																							
ALC A26										R	R	R	R	R	R	R							
ALC A27					R	R	B	B	B	B	B	B	B	B	B	B	R		R	R	R	R	R
YTM A28						R	R	R	R	R	R	R	R	R	R	R							

M/N A29	:												:
M/N A30	:												:
M/N A31	:												:
M/N A32	:												:
M/N A33	:												:
M/N A34	:												:
-------	:												:
2-3 A36	:		R		R	R	R						:
2-3 A37	:		R		R	R	R	R	R	R	R	R	R :
2-3 A38	:												:
2-3 A39	:												:
2-3 A40	:												:
2-3 A41	:												:
2-3 A42	:		R		R	R	R	R	R	R	R	R	R :
2-3 A43	:		R		R	R	R	R	R	R	R	R	R :
-------	:												:
FIL A20	:												:
-------	:												:

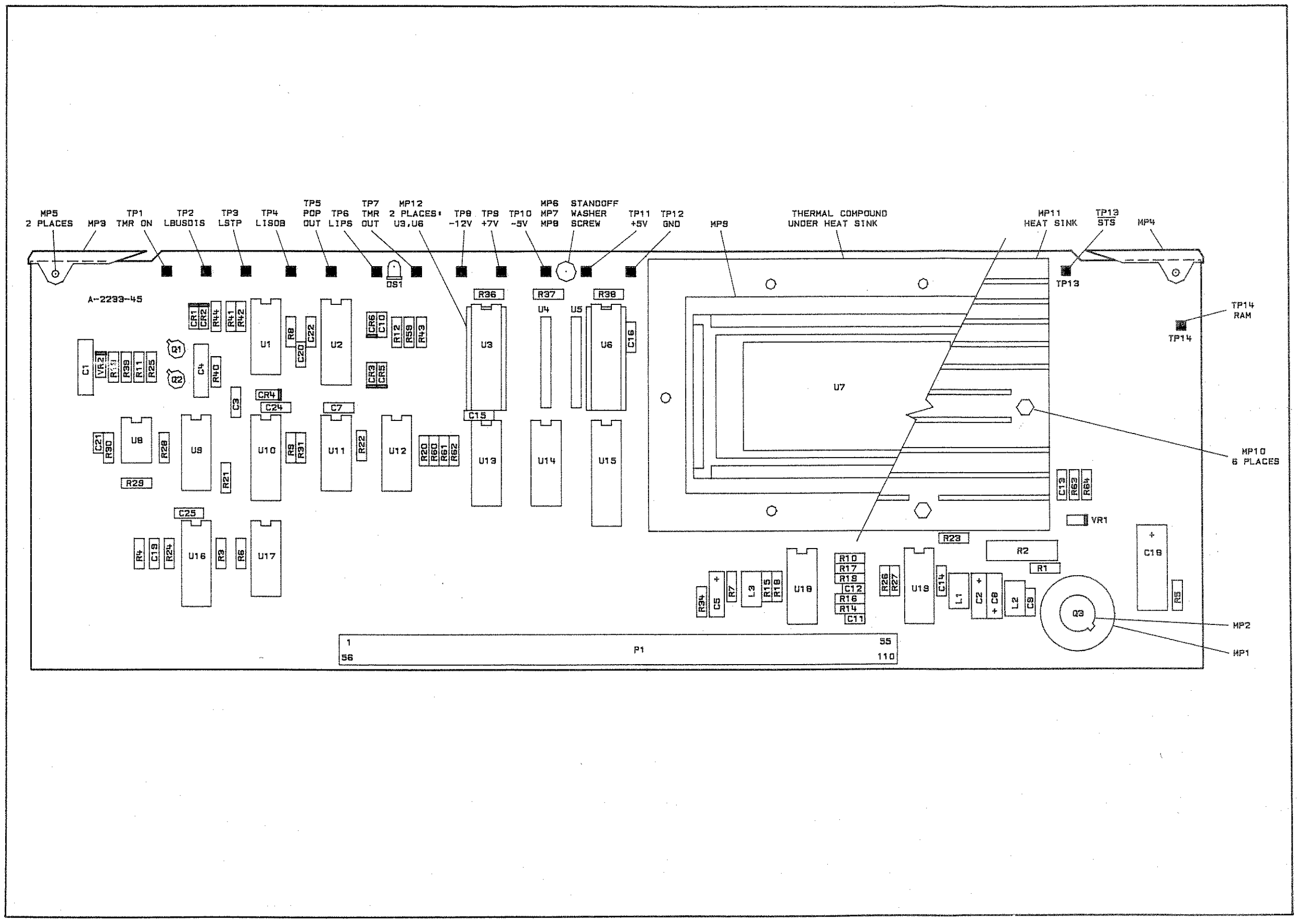


Figure 8-474. A60 Processor, Component Location Diagram

A61 MEMORY ASSEMBLY, CIRCUIT DESCRIPTION

The A61 MEMORY board contains all the firmware (stored in ROM) to run the 8340A and the calibration data and Save/Recall registers (stored in RAM).

The normal sequence of operations is diagrammed in Figure 8-482A.

Figure 8-482A. Memory Operation Timing Diagram.

To be supplied.

1. The processor places an address on the LIDA BUS.
2. The address is latched on the Memory Board by the rising edge of HSTM, (High Start Memory) and the location is accessed.
3. The processor reads data or instruction on LIDA BUS after setting LSOB (Low Stay Off Bus) false (HIGH).
4. The processor executes the instruction or processes the retrieved data word.
5. The processor initiates the sequence once again.

Bus Damper A

Each LIDA BUS line is terminated by a 100 ohm impedance matching resistor (part of U12 or U25) and a diode clamp (part of U13 or U26). This eliminates transient overshoot due to bus impedance mismatch, and protects the inputs from high energy static discharge.

The clamp voltage is generated by Q8 and Q9 in the POWER SUPPLY section (Block H). In this arrangement VCLAMP follows VP, the battery supply to the RAMs. This guarantees that no input to the CMOS RAMs can exceed their VCC value, eliminating the parasitic SCR latch-up problem common to CMOS devices.

Address Latch B

The rising edge of HSTM latches the address on the LIDA BUS into the 16-bit latch U3,U4,U18,U19. Bit 14 selects between ROM and RAM. Bits 12 and 13 select between the 4 pairs of ROM chips. Bits 0 thru 1 select a specific location in a pair of ROM or RAM chips. Due to the specifics of processor architecture, bit 15 does not contain valid address information, and is ignored. The

latched address lines are called the MAR BUS.

Digital Signature Circuit C

This circuit generates the Start and Stop clock signals for a Signature Analyzer during Memory Board testing. A complete description of these tests is given in the A60 Processor documentation.

Shift register U2 is cleared at the start of auto-test software by executing a write to ROM address @03777. A right-shift is forced after each phase of auto-test by executing a write to RAM address @57767.

Note that a write to ROM address @03777 will alter the contents of RAM location @77777, and the write to address @57767 will alter RAM location @77767. This is due to the incomplete decoding scheme used during write operations.

Memory Select D

Decoder U17 uses MAR bits 12 and 13 to select which of the 4 pair of ROMs are to be accessed (LCS1 thru LCS4). During a valid ROM access MAR 14 is LOW (addresses less than or equal to @37777). This line is used to enable the decoder U17 During a RAM access MAR 14 is HIGH (addresses greater than or equal to @40000) and U17 is disabled, pulling all ROM chip select lines (LCS1 thru LCS4) to the HIGH, inactive state. Note that all addresses above @40000 are decoded as valid RAM addresses. HPME is used by the EPROM programmer as a programming strobe, and is not connected in the 8340A. Test point TP5 is the chip select line for the first pair of ROMs, which contain all self-test software. This can be useful during instrument turn-on and troublesooting if Self Test appears to get stuck.

CR6, CR7, and Q4, Q5, Q6, and Q7 decode the VPP/OE' line to the ROMs. This line must go to +25 Volts during EPROM programming, to 0 Volts during a read operation, and to +5 Volts at all other times. VPP/OE' is driven LOW when MAR14 is LOW and LSOB is HIGH. Note that and/or Q4 may be destroyed if the +25 Volt program voltage is present during a read operation to ROM.

Q1, Q2, and Q3 form a discrete NAND gate that is constantly power up by the RAM backup battery. Inputs are the memory cycle strobe HSTM and the LIPS line. A low on LIPS effectively isolates the RAM from invalid Buss activity during instrument power cycling. The output of this gate is the LRAMCE line, tied to the chip select pin on the RAM' Note that every memory cycle, whether to

ROM or RAM, initiates a read cycle in RAM. U16A,B, and C decode MAR14, LWRT, and processor handshake LSOB to drive LRAMEN low true and output RAM contents to the Bus only when a valid RAM read cycle occurs. Also note that, as a consequence of this decoding scheme, a write operation to any location in memory (whether in ROM or RAM space) maps into a write to some location RAM.

ROM E

Eight EPROMs hold all the Main Controller firmware. Each EPROM contains 4096, 8 bit bytes. They are connected in pairs to make up the 16 bit data words required. The total storage space provided in ROM is 16K, 16 bit words. Self-test firmware resides in the first two ROMs, U6 and U21.

The table below details ROM control lines and their states during operation:

	VPP/OE' (20)	CS' (18)	LIDA BUS	MAR BUS
To program EPROMs	+25V	LOW	data in	valid
To read EPROMs	low	LOW	data out	valid
All other times	xx	HIGH	xx	xx

RAM F

System RAM consists of two chips, U5 and U20, each containing 2048, 8 bit bytes, connected in parallel to form the 16 bit data words required. These RAMs are ultra low power CMOS devices. Power dissipation is low enough that at room temperature the on-board battery will maintain data integrity for 10 years. Over the worst case instrument temperature range and RAM current drain data integrity is guaranteed for the normal 1 year instrument calibration interval. Nonvolatility is required because the RAM is used to store instrument calibration data and the Save/Recall registers, as well as stack and normal processor workspace.

The table below details RAM control lines and their states during operation:

	LRAMCE CS',18	LRAMEN OE',20	LWRT	LIDA BUSS	MAR BUSS
To write RAM	LOW	HIGH	LOW	data in	valid
To read RAM	LOW	HIGH	HIGH	data out	valid
All other times	xx	HIGH	HIGH	xx	xx

Note that any write operation (whether in ROM or RAM address space) is mapped into a write to some location in RAM. This includes writes to the Self Test Indicators, and the Digital

Signature Circuit, which are decoded as writes to ROM. The Main Controller is very careful to execute these writes to locations in RAM whose nonvolatility is not required.

Self Test Indicator G

On controller initiation, the LIPS line clears latches U11 and U27. This turns on all indicator LEDs to verify that they are in working order.

The register is loaded by any write to the first block of ROM (locations @00000 to @07777). The Main Controller always uses location @03777, which maps into RAM location @77777. Altering the contents of this location does not compromise the integrity of any nonvolatile data.

A complete description of the coding used for the indicator LEDs is given in the A60 Processor Documentation.

Power Supply H

+5VF is the instrument main 5V power supply. It is decoupled at the edge connector by L1 and C20 to isolate current spikes,. generated by Memory Board operation, from the rest of the instrument.

+25VPP (PGM) is the programming potential required by the EPROMs during programming, and is provided by the EPROM programmer. Except during programming this line must be at +5 Volts. In the 8340A the PGM line is tied directly to the +5V main supply on the Motherboard.

+5VP is the CMOS RAM VCC line. To maintain nonvolatility of RAM contents, on board batteries maintain +5VP at or above 2.0 Volts. The RAMs, then, are always powered up, even when the board is removed from the instrument. Careful handling of the Memory board is a must. The first rule is: Never set the board on a conductive surface - you may short +5VP to ground.

Batteries BT1 and BT2 are connected to +5VP thru steering diodes CR1 and CR2. While the instrument is in STANDBY mode (and connected to a live AC mains) the +22V power supply is up. All other supplies are powered down. Resistor R9 and zener diode VR1 drop the +22V in to 5.11V and the +5VP line is sourced from this regulator. CR3 is reverse biased in STANDBY and has essentially 0V across it when the instrument is ON (and the +5V supply is up). Its purpose is to ensure that the +5VP line tracks the main +5VF supply in the event of a failure in the +22V standby supply. Note that shorting +5VP to ground while +5VF is active will destroy CR3. The batteries supply +5VP at about +2.5V only when

the instrument is disconnected from the AC mains, or the Memory Board is removed from the instrument.

To ensure RAM integrity for the 1 year instrument calibration interval, total battery current (sum of currents from BT1 and BT2) must not exceed 19uA. Battery current is determined by measuring the voltages across R1 and R2:

$$I(batt) = V(R1)/51.1 + V(R2)/51.1 .$$

If the current drain exceeds 19uA, usually one of the RAMs or one of the VMOS FETs (Q1, Q2, Q9) is defective and must be replaced.

Because RAM contents are guaranteed only when VCC is greater than or equal to 2.0 Volts, a battery is considered fully discharged when the voltage measured directly across it reaches 2.2 Volts. Regardless of their apparant state of charge, batteries should always replaced and their current drain measured when the instrument is calibrated. This is necessary to guarantee retention of calibration factors for the 1 year normal calibration interval under worst case conditions.

Q9 is a source follower set to track the backup supply +5VP. It then sets the potential at the base of the active clamp Q8. Clamp voltage VCLAMP will always be low enough to ensure that no RAM input line will exceed its VCC (+5VP). This eliminates the parasitic SCR latchup problem inherent in CMOS devices.

In normal operation VCLAMP is required to sink current only. However, during a very fast LIDA BUS transition from HIGH to LOW, charge pump due to the junction capacitance of the clamp diodes (part of U13 or U26) requires VCLAMP to source current for a short time. C23 lowers VCLAMP output impedance, and allows it to source the required current without changing the clamp level.

The clamp circuit is easily tested by sourcing current into it (connect a 347 ohms resistor from the +12V instrument supply to the VCLA line at some point), and measuring its compliance. VCLAMP at 20mA not exceed +3.9 Volts, and the change in clamp voltage from ICLAMP=0 to ICLAMP=20mA should not exceed 0.20Volts.

SIGNAL LIST AND DICTIONARY

LIPS	Low Instrument PreSet
HSTM	Hi STart Memory
LCS1-4	Low Chip Select 1-4 selects one of 4 pairs of ROMs
LSOB	Low Stay Off the Buss
LRAMCE	Low RAM Chip Enable
LRAMEN	Low RAM output ENable
LIDA0-15	Low Instrument Data and Address Bus bit 0-15

MAR0-15	Memory Address Register bus bit 0-15
LWRT	Low WRiTe
T0-3	Test clock bit 0-3 signature analyzer clocks
VPP/OE'	Program Voltage / Output Enable for ROMs
HPME	High PrograM Enable

MEMORY MAP

	OCTAL ADDRESS FIRST	LAST
ROM U6,U21	00000	07777
ROM U7,U22	10000	17777
ROM U8,U23	20000	27777
ROM U9,U24	30000	37777
RAM U5,U20	74000	77777

TROUBLESHOOTING

Troubleshooting for the A61 Memory Board is included along with the A60 Processor Board documentation.

Note: Calibration factors, stored in RAM, are required to meet instrument performance specifications. While loss of cal data does not impair the physical operation of the instrument, the loss in performance must still be considered an instrument failure.

Several situations have been identified that can cause the loss or alteration of RAM contents:

1. Placing the board, component side up, on a conductive surface (ie metal benchtop, screwdriver,...)

2. Shorting the main +5V power supply to ground when the +12V supply is active causes a glitch on the HSTM strobe. Occasion- ally the LWRT line will drop to the valid LOW threshold on the RAM (VIL) before HSTM has returned LOW. This executes a write the RAM location pointed to by the address latch.

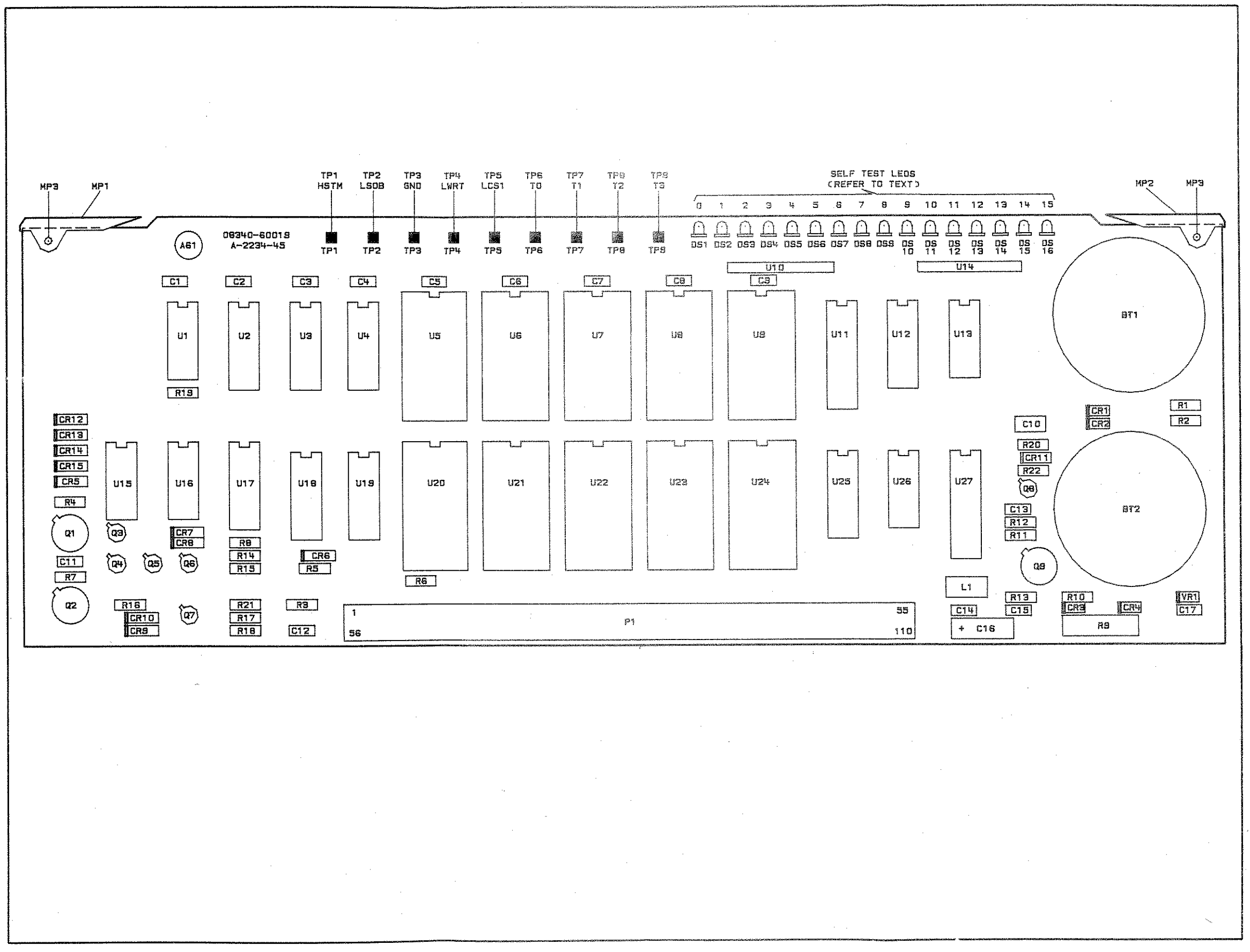
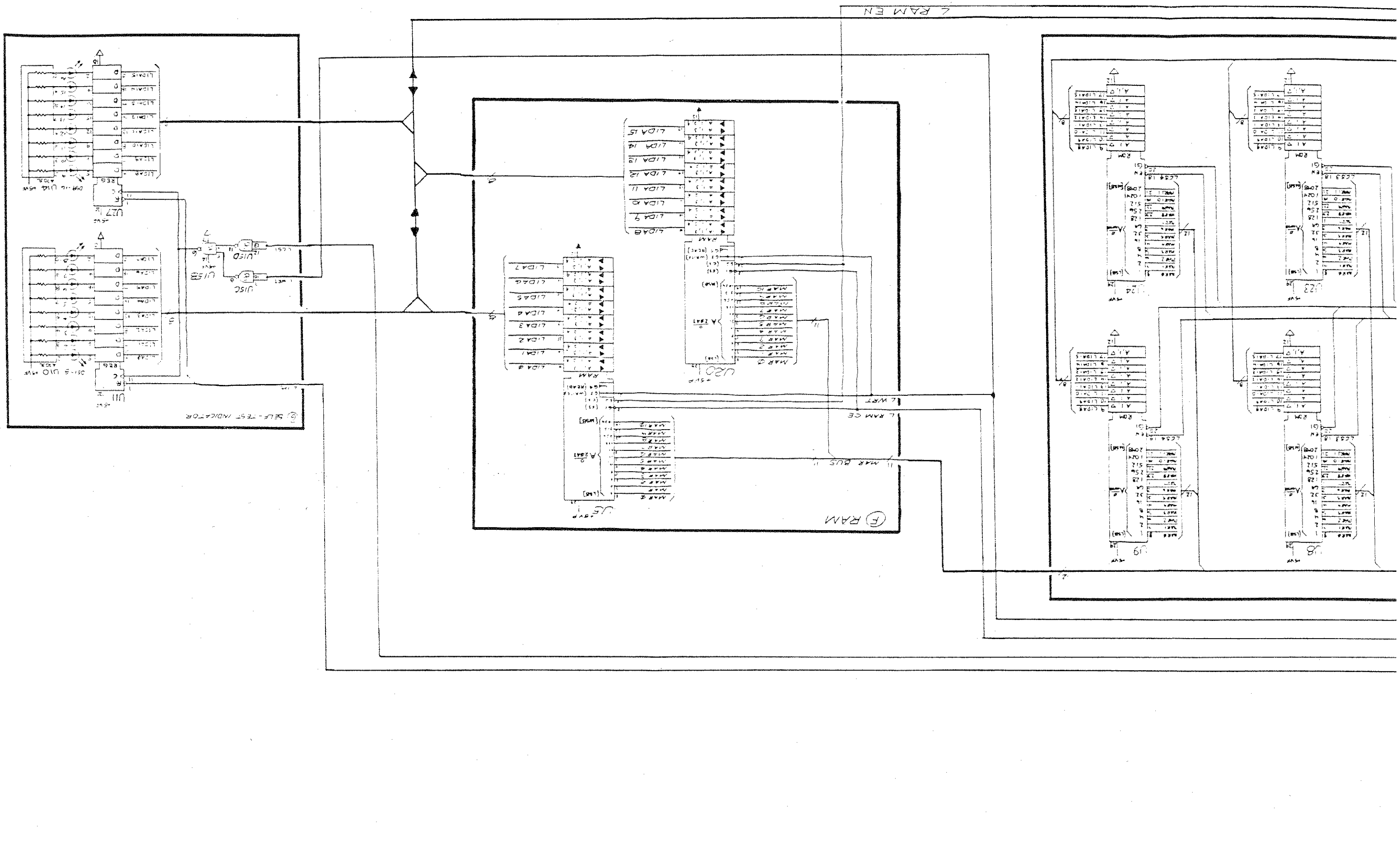


Figure 8-486. A61 Memery, Component Location Diagram

A61 MEMORY
08340-60019

SERIAL PREFIX: A-2237-45

28 SEPT 82


Ⓕ RAM
Ⓖ SELF-TEST INDICATOR
RAM
ROM
MAR BUS
L RAM CE
L WRT
L RAM EN

NOTES

1. REFER TO FIGURE 8-X FOR DETAILED SCHEMATIC DIAGRAM NOTES.

2. RESISTANCE VALUES ARE IN OHMS, CAPACITANCE IN MICROFARADS, AND INDUCTANCE IN MICROHENRIES UNLESS OTHERWISE NOTED.

3. +25Vp-p (PGM) IS THE PROGRAMMING POTENTIAL REQUIRED BY THE PROMS. THIS LINE IS NORMALLY AT +5 VOLTS. REFER TO TEXT.

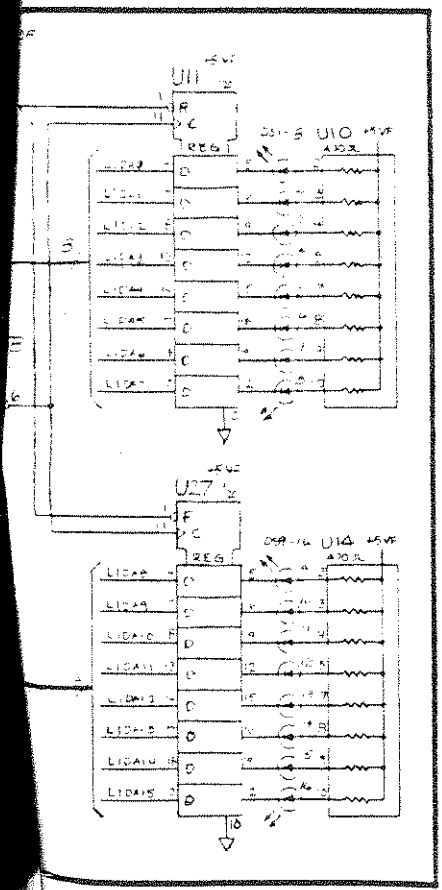
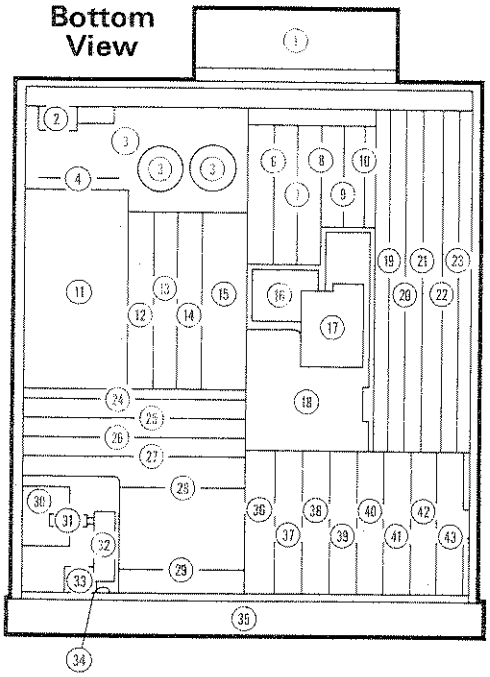
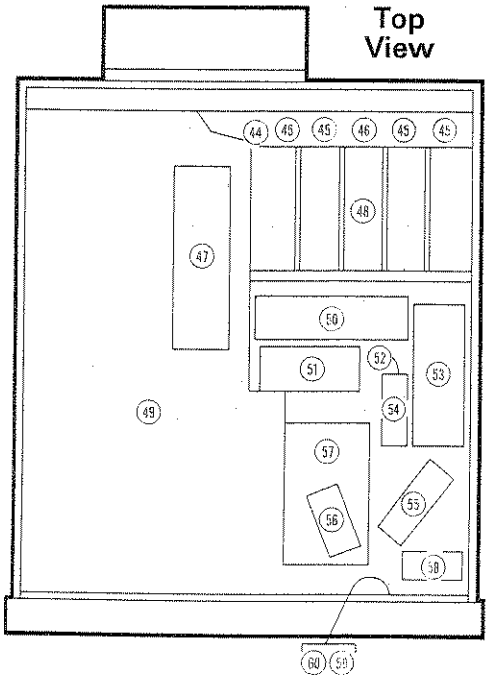


Figure 8-488. A61 Memory, Schematic Diagram

REFERENCE GUIDE TO SERVICE DOCUMENTATION





Assy./Ref. Des.	Description	Location	Volume 2					Volume 3	
			Ref.-M/N Loops	20/30 Loops	Swp. Gen.-YO Loop	Motherboard	Controller	Front/Rear Panel	RF Section	Power Supplies
A1	Alpha Display	35					•			
A2	Display Driver	35					•			
A3	Display Processor	35					•			
A4	Not Assigned	-								
A5	Keyboard	35					•			
A6	Keyboard Interface	35					•			
A7	Lower Keyboard	35					•			
A8	3.7 GHz Oscillator	57						•		
A9	Band 0 Pulse Modulator	56						•		
A10	Directional Coupler	52						•		
A11	Band 1-4 Detector	31						•		
A12	Band 0 Detector	34						•		
A13	SYTM (Switched YIG Tuned Multiplier)	50						•		
A14	Band 1-4 Power Amplifier	53						•		
A15	Band 0 Low Pass Filter	52						•		
A16	Band 1-4 Modulator/Splitter	51						•		
A17	Band 0 Mixer	54						•		
A18	Band 0 Power Amplifier	55						•		
A18A2	Band 0 Splitter	60						•		
A19	Capacitor Assembly	48							•	
A20	RF Section Filter	50						•		
A21	Pulse Modulator Driver	49						•		
A22	Not Assigned	-								
A23	Not Assigned	-								
A24	Attenuator Driver/SRD Bias	28						•		
A25	ALC Detector	27						•		
A26	Linear Modulator	26						•		
A27	Level Control	25						•		
A28	SYTM Driver	24						•		
A29	Reference Phase Detector	7	•							
A30	100 MHz VCXO (Voltage Controlled Crystal Osc.)	12	•							
A31	M/N Phase Detector	4	•							
A32	M/N VCO (Voltage Controlled Osc.)	15	•							
A33	M/N Output	15	•							
A34	Reference-M/N Motherboard	15	•							
A35	Rectifier	4							•	
A36	PLL1 VCO (Voltage Controlled Osc.)	36		•						
A37	PLL1 Divider	37		•						
A38	PLL1 IF	38		•						
A39	PLL3 Upconverter	39		•						
A40	PLL2 VCO (Voltage Controlled Osc.)	40		•						
A41	PLL2 Phase Detector	41		•						
A42	PLL2 Divider	42		•						
A43	PLL2 Discriminator	43		•						
A44	YIG Oscillator (YO)	8			•					
A45	Pre-Leveler	15			•					
A46	7 GHz Low Pass Filter	16			•					
A47	Sense Resistor Assembly (YO circuit) (SYTM circuit)	47 47			•			•		
A48	YO Loop Sampler	18			•					
A49	YO Loop Phase/Detector	18			•					
A50	YO Loop Interconnect	17			•					
A51	Reference Oscillator	16	•							
A52	Positive Regulator	5							•	
A53	Negative Regulator	5							•	
A54	YO Pretune DAC/Delay Compensation	8			•					
A55	YO Driver	9			•					
A56	-15V Regulator	10							•	
A57	Marker/Bandcross	19				•				
A58	Sweep Generator	20			•					
A59	Digital Interface	21				•				
A60	Processor	22				•				
A61	Memory	23				•				
A62	Main Motherboard	58					•			
A63	70 dB RF Attenuator	59						•		
AT1	Peripheral Mode Isolator	56						•		
B1	Fan Assembly	1							•	
A62C1-3	Power Supply Filter Capacitors	3							•	
FL1	AC Line Module	2							•	
A62Q1-4	Power Supply Regulating Transistors	-							•	
A62S1	Power Supply Thermal Switch	44							•	
T1	Power Supply Transformer	11							•	
A62U1	Power Supply Regulator	46							•	

FRONT PANEL — REAR PANEL

DISPLAY SECTION, CIRCUIT DESCRIPTION

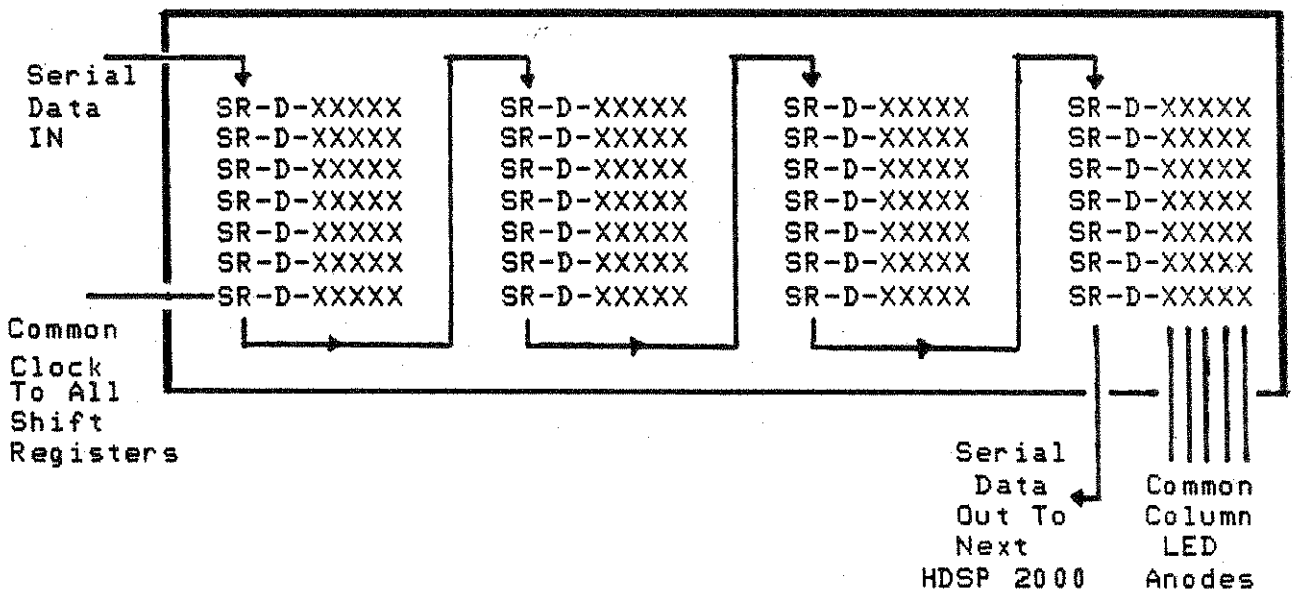
Introduction

The Display Section includes the A1 Alpha Display Assembly, the A2 Display Driver Assembly, and the A3 Display Processor Assembly.

Each of the three assemblies are documented individually in the following descriptions. Troubleshooting information follows the circuit descriptions.

A1 ALPHA DISPLAY, CIRCUIT DESCRIPTION

The HDSP 2000 integrated 5X7 dot matrix display is used in the 8340A for display of alphanumeric information. Seven four character chips are used for a total of 28 characters. The shift registers (SR), drivers (D) and LEDs (X) are arranged as follows:



When the processor is ready to display a line in the alpha display, the processor first fetches the character in the last character position out of RAM. Next the processor determines which column of the alpha display it is setting up. Then the 1/0 patern for that character in the row determined is looked up in a table and written to the serial shift register. These ones and zeros are shifted into the alpha displays. The processor now goes back and gets the character for the next to the last position and repeats the above sequence. Once all 196 (7X28) bits have been shifted into the displays, all of the selected LEDs in one of the five columnn by pulling HIGH on the appropriate column line. The above sequence is repeated for each of the five columns and the whole process is repeated at a rep-rate of approximately 80 times per second to insure a flicker free display.

The alpha display shift clock is the same alpha display clock generated and controled on the Display Processor Board. The alpha displays dissipate a lot of power and as a result they must be heat sunk very well. For this reason the display chips are soldered into the PC board and the PC board is screwed directly to the anodized aluminum bezel assembly. On the P.C. board, all of the pins to the chips have as much copper connected to them as possible so that the heat will be conducted into the copper on the PC board and then into the bezel. Heat sink compound should be used between the alpha display

PC board and the bezel to insure a low thermal resistance.

A2 DISPLAY DRIVER BOARD, CIRCUIT DESCRIPTION

Numeric Segment Drivers A

Each numeric digit is formed by various combinations of seven segments and a decmial point. The anodes of the same segment in each numeric digit are connected in parallel and go to a segment driver. The cathodes of all eight segments within a digit are connected in parallel and go to a digit driver. Therefore, there are eight segment drivers common to all digits plus one digit driver for each of the 31 digits. To display numbers in all display digits, the processor starts at the first digit by clearing the segment driver latch and by turning on the digit driver for the first digit. The display processor then determines from RAM what character should be displayed in this first digit and then sets the appropriate bits of the segment driver latch. Once these bits of the latch are set, the corresponding segment drivers supply current thru the segment and out the digit driver. The processor leaves these drivers on for a few tens of mili Seconds. At the end of this display time, the segment drivers are all turned off. The shift register/digit driver is immediately shifted to drive the second digit. None of the LED segments of the second digit turn on until the processor determines what character should be displayed and turns on the appropriate segment drivers. This second digit is then displayed for a few tens of mili Seconds and so on thru all 31 digits until the last digit is displayed and then the whole process is started over. This whole process is repeated about 80 times per second so the eye is not able to perceive the flicker.

The processor selects which numeric segments to turn on by setting the approprite bits in a 74LS259 8 bit addressable latch (U9). Processor I/O port P14 thru P17 (A3U1 pins 31 thru 34) control the address and D input to the NE591 (U9). The address bits (U9 pins 1,2 & 3) are set to indicate the bit in the latch being changed and the D input (U9 pin 13) is set HIGH or LOW depending on whether you wish to turn on a segment or turn off a segment. The clock line (U9 pin 14) is connected to the processor ALE line through a NAND gate which will cause this clock to be HIGH anytime reset is TRUE. Since this clock is essentially the same as the processor ALE line, each instruction cycle the information currently contained on the address and D inputs will be transferred to the outputs of the addressable latch (U9 pins 4 thru 7 & 9 thru 12).

Each output of the addressable latch (U9) is connected thru a 1K ohm resistor to a segment current source and to a 2.2 K ohm resistor connected to the main +5.2 v supply.

The segment current sources are formed by two transistors and a

resistor (Q11,Q12 & R29 for example). When the addressable latch output (U9 pin 12) goes HIGH, the upper transistor (Q11) is turned on due to the base current supplied by the 2.2 K ohm resistor and conducts current from the display supply out its emitter and thru the resistor (R29). This current increases until the voltage drop accross the resistor (R29) equals the VBE drop of the lower transistor.

As soon as this current is reached, the lower transistor (Q12) begins to conduct and removes some of the base drive current to the upper transistor (Q11). This process reaches an equilibrium with the lower transistor (Q12) conducting just enough current to remove the excess base current supplied to the base of the upper transistor (Q11). This type of current source is used because it is fairly immune to the voltage variations of the display supply. Note: (current doesn't flow until the numeric digit driver is on.)

When the addressable latch output (U9 pin 12) goes LOW it conducts all of the current provided by the 2.2 K ohm resistor away from the base of Q11 thus turning off the current source.

Each of the eight segment current sources provides approximately 0.60/16.2 or 37 mA to its particular segment.

Numeric Displays B, C And D

The numeric displays consist of two 15 digit and 5 digit monolithic seven segment displays (A matched set is available to provide equal illumination). In the 8340A, only 13 of the 15 digits are used in each of the larger displays.

LED Annunciators E

Each annunciator is connected in series with a current limiting resistor to +12 volts. The resistor values are selected to make the apparent brightness to the eye the same on all annunciators.

Level Shifters F

In order to meet the input voltage requirements of U4, U5 and U8 power shift registers (Block G), level shifters are used to translate the TTL levels to that required by these ICs.

When the input to the clock level shifter (R7,R8,R9,VR4 and Q6) is not pulled LOW, current is supplied to the base of Q6 thru R9 and VR4 and thus causes Q6 to turn on. When Q6 turns on it pulls one end of R7 down to approximately -5 volts. Each clock input sources 1.8 to 3.5 mA; therefore, the current thru R7 will be between 5.4 and 10.5 mA making the voltage at the clock inputs

(U4, U5 & U8 pin 9) between -3.6 and -2.25 volts. When the input to the clock level shifter is LOW, base of Q6 is allowed to be pulled down to -5.2 volts thus turning Q6 off and allows the internal pullups of the IC to pull the input HIGH. When the input to one of the start level shifters (R1,R2,VR1 or R3,R4,VR2 or R5,R6,VR3) is not pulled LOW, the start input (U4, U5, & U8 pin 8) will be at approximately +.6 volts. When the input to one of the start level shifters is pulled low (1.0 volts), the start input will be at approximately -2.2 volts due to the 3.16 volt differential supplied by the zener diode (VR1, VR2 or VR3).

Shift Register/Numeric Digit Driver G

The numeric digit drivers (U4, U5 & U8) are power shift registers whose outputs are capable of sinking 250 mA. When the start line (pin 8) is pulsed HIGH, all outputs of the shift register (pins 11 thru 20 & 1 thru 7) go HIGH. After the application of a start pulse, the first LOW going clock pulse applied to the clock line (pin 9) will cause output Q15 (pin 11) to go LOW. Each successive pulse on the clock line (pin 9) shifts this low output to the next stage and the previous stage output goes HIGH. The LOW output shifts thru each stage and finally is shifted out of the shift register at which time all outputs will again be HIGH. The outputs of these power shift registers (U4, U5 and U8) are each connected to all the segment cathodes of one digit thus when the output goes LOW it turns on all of the segments in that digit whose segment drivers are activated. The power shift registers have non-standard logic levels for the clock and start inputs. The clock input (pin 9) LOW level is -2.2 volts and has a pull up inside the IC so it can be driven from an open collector transistor. The start input (pin 8) has a HIGH level of +.5 volts and a LOW level of -.8 volts.

Control Data Latch H

The control data latch (U3) is A NE590 open collector addressable D-latch. The address inputs (U3 pins 1,2 and 3) and the D input (U3 pin 13) are connected to the display processor I/O port P10 through P13 (A3U1 pins 27 through 30). The clock line (U3 pin 14) is connected to the ALE signal so with each ALE cycle the latch will be updated with the current information contained on the I/O port lines. Outputs 4,5 & 7 (U3 pins 9, 10 and 12) go to the numeric display start pulse level translators. Outputs 0,1,2,3 and 6 (U3 pins 4,5,6,7 and 11) go to Alpha display column drivers 3,2,1,4 and 5 respectively.

Alpha Column Drivers I

The alpha column drivers are formed by Q1 thru Q5 and resistor packs U1 and U2. When it is time for the processor to turn on on

of the alpha columns, the processor addresses one of the column control lines in the control data latch (U3) LOW which pulls down on the base of one of the column driver transistors (Q1 thru Q5) thru a 24 ohm resistor. This turns on the transistor which pulls the column line up to the Display Supply.

A3 DISPLAY PROCESSOR, CIRCUIT DESCRIPION

Instrument Bus Interface A

The INSTRUMENT BUS INTERFACE consists of an eight bit D-latch (U6) and a 3-8 line decoder (U10).

The 3-8 line decoder (U10) decodes I/O strobes from the instrument address bus and the SIOA signal. I/O channel 15,R0: (I/O channel 15,R0: is channel 15 sub channel 0. Refer to A61 Processor description for more channel/sub channel information) (U10 pin 10) latches annunciator control bits (Block C) off the instrument data bus. I/O channel 15,R2: (U10 pin 7) is the interrupt strobe to the display processor and the clock to the 8 bit D-latch (U6 pin 11) which latches the data being sent to the display via the instrument data bus.

The 8 bit D-latch serves to connect the two asynchronous buses together. The Q outputs of this latch are connected to the displays internal data/address bus. When the display processor is ready to accept the data stored in the input latch (U6), the read line of the processor (U1 pin 8) goes low enabling the D-latch (U6 pin 1) which then outputs onto the display data bus.

Service Request Latch

This latch consists of two nand gates connected as a set/reset latch. Nand gate #1 has both of its inputs(U3 pins 1 & 2) HIGH so its output (U3 pin 3) will be LOW. Nand gate #2 has one input (U3 pin 4) connected to the output of nand gate #1 (U3 pin 3) which is LOW. The other input (U3 pin 5) is connected to the processor read line (U1 pin 8 Block B) which is HIGH until it reads the data contained in the 8 bit data bus latch (U10). The output of nand gate #2 (U3 pin 6) is therefore HIGH which makes the circuit stable in this state until some input changes.

When the instrument processor sends an interrupt to the display, the interrupt line (U10 pin 7) goes LOW and then HIGH 400 nS later. When this line goes LOW, U3 pin 1 goes LOW which causes the output of nand gate #1 to go HIGH. This forces U3 pin 4 to go HIGH which causes the output of nand gate #2 (U3 pin 6) to go LOW. When this output goes LOW it forces the other input to nand gate #1 (U3 pin 2) LOW which makes the circuit stable in this state until some input changes. This output (U3 pin 6) is also connected to the interrupt line of the display processor (U1 pin 6). When this pin goes low, the processor starts an interrupt sequence.

During the interrupt service routine, the display processor takes the read line (U1 pin 8) LOW which is connected to an input to

nand gate #2 (U3 pin 5) and to the 8 bit data bus latch (U6 pin 1). When this happens, the output of nand gate #2 (U3 pin 6) goes HIGH which forces one input to nand gate #1 (U3 pin 2) HIGH. If the other input to nand gate #1 is HIGH (U3 pin 1 interrupt strobe) the output of nand gate #1 (U3 pin 3) will go LOW which presents a LOW at U3 pin 4 and makes the circuit stable in this state until some input changes and this completes the cycle.

Display Processor B

The display processor is a 8049 micro-computer. It contains 128 bytes of RAM and 2K bytes of ROM program memory. This ROM contains all of the microcoded program to control the display processor. It contains an 8 bit down counter which uses a prescaled (divided by 32) ALE signal for its input clock. I/O consists of two 8 bit parallel ports which can be either input or output. The bi-directional data bus has both data and address information multiplexed onto it.

The display uses the 128 bytes of RAM for internal registers, storage for the present characters being displayed in the numeric and alpha displays and for a Command First In First Out Register (FIFO).

The instrument processor communicates with the display processor via 16 bit bi-directional bus, however, the display processor cannot send data back to the instrument processor. The instrument processor places command or data information on the instrument data bus and then strobes the display interrupt. The display processor immediately takes the information present on the data bus and places it on the bottom of the FIFO. Commands and data contained on the FIFO are executed sequentially when the display processor has time that is not required to refresh the numeric and alpha displays. This method provides the minimum response time to interrupts from the instrument processor and at the same time always provides flicker free display refreshing.

The oscillator circuit consists of a 10.92 MHz crystal connected to the internal oscillator circuit of the processor (pins 2&3). A crystal is used rather than an LC circuit due to variations in oscillator frequency from unit to unit when a LC circuit is used. (Refer to an Intel 8039 data sheet for a more detailed discussion of the processor.)

U3C provides a clock signal to the two control Addressible Latches on the display driver board (A2). This clock line is required to be HIGH when the reset to these Addressable Latches is LOW so LOW Reset is NANDed with the ALE clock to force the above condition to occur.

Annunciator Latch/Driver C

When the annunciator strobe goes low and then high (U5 & U7 pin 9), the information on the instrument data bus is latched into the annunciator data latches. The outputs of these latches drive the inputs of the annunciator drivers (U4 & U8). The annunciators are located on the A2 Display Driver Board. Each annunciator is connected in series with a current limiting resistor to +12 volts. The resistor values were selected to make the apparent brightness to the eye the same on all annunciators. The High Voltage drivers (U4 and U8) provide sufficient current sink capability and allow the use of the +12 volt supply for the annunciators.

Preset Circuitry D

The preset circuitry has two purposes. The first is to allow the instrument preset signal to clear the annunciator LEDs and to reset the display processor. The second is to allow either the instrument preset signal or the display processor to clear the numeric display segment driver data latch.

The LIPS signal comes into the display to a schmitt trigger buffer (U9B pin 5) is inverted twice and appears at U9 pin 3 with polarity unchanged. This buffered LIPS directly clears the annunciator latches (U5 & U7 pin 1 in Block C) and directly resets the display processor (U1 pin 4 in Block B). This LOW true signal is or'ed (U9D pin 12 and 13) with a LOW true signal from I/O Port P25 of the display processor (U1 pin 36). The output of the above gate (U9D pin 11) is inverted (U9C pin 10) to produce the low true clear (U9C pin 8) to the A2 Numeric Segment Driver data latch Block A.

DSA Connector E

Start, Stop, Clock and Ground are arranged in the same order as on the Signature Analyzer pod. The DSA function is enabled by shorting the Gnd and DSA Enable lines on the DSA connector (TP5 and TP6) together and forcing the LIPS line LOW (momentarily) by pressing instrument preset or momentarily shorting LIPS to ground on the display.

Two additional pins (TP7 and TP8) are connected to +5.2 volts and the 8039 processor's External Access (EA) pin. When this pin is tied to +5.2 V it forces the processor to do all instruction fetches from external memory. This function may be useful for trouble shooting address/data bus problems.

Alpha Display Shift Register F

The alpha displays require row information in serial form. This shift register (U2) has its parallel inputs (U2 pins 3,4,5,6,12,13 and 14) connected to the display data/address bus. When the display processor does a write, the write line (U1 pin 10 in Block B) goes LOW and forces the parallel load line (U2 pin 1) LOW which loads the data on the data bus at that time into the shift register (U2). This information is then shifted serially to the A2 Alpha Column Drivers Block I.

Alpha Display Clock Control

The alpha display clock syncronizes the transfer of serial data from the alpha display shift register (U2) into the serial shift registers contained within the alpha display integrated circuits.

The main sequence synchronization clock (ALE) is Anded (U3D pin 12 and 13) with I/O Port P27 from the display processor (U1 pin 38) to produce the alpha display clock signal (U3D pin 11). This signal goes to the shift register (U2 pin 2) and to the A2 Alpha Column Drivers (Block I) and allows the display processor to control the number of bits shifted into the Alpha Display. This method of genterating a clock produces the fastest transfer of serial information to the Alpha Displays and allows the processor to do other things, once the shift clock has been turned on, until it is time to turn the clock off.

Display Supply G

The peak current required by the displays can be as high as 2 amps; however, the average current required is much less. These current peaks or transients caused by strobing the Alpha and Numeric displays cause spurs on the 8340A RF output.

A constant current source connected to the instrument +5.2 volt supply is provided so that a constant load will be seen by the instrument supplies. The output of this current source is then connected to the LED current source circuits along with a large amount of energy storage (5 220 uF capacitors). The current source provides slightly more than the average amount of current required by the LEDs, and the capacitors provide the additional current required during peak demands.

Q1, Q2, and U11B form the display current source. Q1 and Q2 increase the current capability of the current source. If you disregard U11A for the moment then the emitter of Q1 will be forced to the same voltage as the positive input of U11B by virtue of the voltage feed back thru R9. The positive input (U11B pin 5) is fixed at one diode drop below the supply (+5.2VF). R5 therefore, has a constant voltage drop accross it and produces the constant current for the display supply. The average current

demanded by the displays changes as more or less segments or characters are turned on. In order to keep the current source in regulation during both high and low average current demands it is necessary to make the current source adjustable. This is accomplished by sensing the voltage at the energy storage capacitors thru R11. As this voltage goes down, indicating that the average current is not sufficient, the voltage at U11A pin 1 will go up which will cause an increase in the voltage accross R5 and therefore will increase the current to the display supply. It would not be desirable to have the current source track the voltage at the output and respond to the variations due to strobing the various segments and columns since this would defeat the whole purpose of the current source so U11A is connected as a slow integrator. It responds only to slow variations in the average voltage at the display supply. R12 and R13 set the quiesent operating point of the current source. R11, R3 and C20 set the gain and speed of the integrated voltage feedback loop.

When the current source has been supplying a relatively large amount of current and suddenly the requirement goes down drastically, the current source will try to continue supplying this large current and therefore the voltage at the output will rise until it cannot go any higher and then the current source will go out of regulation causing a current transient on the main supply to the display. VR1 and R6 are used to sink this excess current until the integrating feedback has time to reduce the average output current.

Power Supplies H

The power supply filtering is pretty straight forward except for the choke (L2) in the +5.2 volt supply line. The intention of this choke is to further filter out conducted transients on the 5 volt supply caused by the processor, TTL circuitry and other display circuitry that could not be connected to the current regulated supply due to the voltage variations of that supply. Spurs related to the display processor running are reduced by approx 15 dB by adding this lossy filter choke.

DISPLAY ASSEMBLY DSA TROUBLESHOOTING

A. Overview of DSA Options

1. OPTION 1 -
The display processor can be forced to repetitively count through its entire address space. A signature analyzer can then be used to determine if the correct signatures appear on the ADDR/DATA buss.

2. OPTION 2 - The DSA routine contained in the display processors memory can be used by enabling the DSA mode and using a signature analyzer to determine if the correct signatures appear on the Addr/Data buss, the Latched Address Bus, the Parallel I/O Ports and many other signal lines. This routine is not able to check the annunciator latches or drivers, the instrument bus interface latches or any of the signals on the display driver board which have non-TTL levels.

3. OPTION 3 - The instrument DSA routine can be used to stimulate the annunciator latches, the address decoder and the instrument bus interface latch. A signature analyzer may then be used to determine if the correct signatures appear on these lines.

B. OPTION 1 -- FREERUN DSA

The Freerun DSA mode is selected by connecting EA (T.P. 7) to +5.2 V (T.P. 8). This forces the processor to do all instruction fetches from external memory. Since there is no external memory and the Addr/Data bus is pulled up, the processor will fetch FF Hex instruction op codes which does not alter the program counter. After executing this instruction the processor will increment its program counter and do an instruction fetch from the next location and will therefore repetitively count through its entire memory space.

In order to use DSA under the above conditions, the signature analyzer must be connected as follows:

START and STOP connected to A10 (U1 pin 23).
trigger on falling edge

CLOCK connected to LE (U3 pin 8)
trigger on leading edge

After connecting as described above, the Signature Analyzer may be used to check for the correct signatures on all of the Addr/Data bus lines.
If the correct signatures are obtained at the connector to the memory board (J1), this indicates that the Addr/Data bus is functioning correctly and none of the lines are shorted high or low or to each other.

The correct signatures under the above conditions are:

Addr/Data	J1 pin #	Signature
0	11	H62U
1	10	C21A
2	9	HA07
3	8	H0AA
4	7	P030
5	6	4442
6	5	4U2A
7	4	0772
8	1	9635
9	2	1734
10	3	8P54
+5.2 V	17	7A70

C. OPTION 2 -- DSA Using The Routine Contained in Display Memory

The internal DSA routine is enabled by shorting the DSA enable line (T.P. 5) to ground (T.P. 6). The signature analyzer must be connected as follows:

START connected to T.P. 1
STOP connected to T.P. 2
CLOCK connected to T.P. 3 trigger on rising edge
GRND connected to T.P. 4

Set the START polarity to trigger on the falling edge.
Set the STOP polarity to trigger on the leading edge.

The +5.2 V Signature under these conditions should be H9U2. This indicates that all processor instructions are being executed correctly, the ROM check sum is correct and that the internal RAM is good.

Set the START polarity to trigger on the leading edge.
Set the STOP polarity to trigger on the falling edge.

The following table lists the valid signatures for all the signals that can be tested using this DSA option.

SIGNAL NAME	LOCATION	SIGNATURE
D0	U1 pin 12	CPAC
D1	U1 pin 13	20U1
D2	U1 pin 14	5P21
D3	U1 pin 15	8F24
D4	U1 pin 16	FP86
D5	U1 pin 17	023P
D6	U1 pin 18	185F
D7	U1 pin 19	H576
P10 (NE590 A)	U1 pin 27	C606
P11 (NE590 B)	U1 pin 28	06F6
P12 (NE590 C)	U1 pin 29	5868
P13 (NE590 D)	U1 pin 30	39C4
P14 (NE591 C)	U1 pin 31	H2A6
P15 (NE591 D)	U1 pin 32	5FC3
P16 (NE591 B)	U1 pin 33	3U26
P17 (NE591 A)	U1 pin 34	PP24
P20 (A8)	U1 pin 21	4218
P21 (A9)	U1 pin 22	162P
P22 (A10)	U1 pin 23	131U
P23 NOT USED		
P24 (DSA START)	U1 pin 35	F81C
P25 (CLEAR)	U1 pin 36	CH4A
P26 (NUM CLOCK)	U1 pin 37	20PA
P27 (CLOCK EN)	U1 pin 38	0H8P
ALPHA SHIFT CLK	U3 PIN 11	F81C
CLR NOT	U9 pin 11	7551
CLR	U9 pin 8	CH4A
DATA	U2 pin 9	F033
LVL START	60009 U3 pin 9	36PH
F1 START	60009 U3 pin 10	324H
F2 START	60009 U3 pin 12	5746
LAB0	60006 U2 pin 2	7343
LAB1	60006 U2 pin 5	CF6P
LAB2	60006 U2 pin 6	69CH
LAB3	60006 U2 pin 9	UH79
LAB4	60006 U2 pin 19	P061
LAB5	60006 U2 pin 16	AAP4
LAB6	60006 U2 pin 15	8F2P
LAB7	60006 U2 pin 12	F6AH

D. OPTION 3 -- DSA Using the Instrument DSA Routine
The 8340A main processor has incorporated a general purpose DSA routine which exercizes all of the I/O addresses. This can be enabled by connecting STS test point on the processor to ground. The signature analyzer should be connected as follows:

START connected to TP1 on the memory board
trigger on the rising edge

STOP connected to TP t2 on the memory board
trigger on the rising edge

CLOCK connected to TP IOSB on the processor board
trigger on the rising edge

GRND connected to chassis or ground pin

When the instrument is turned on, the instrument will continually send out signatures to each output address. The information contained on the data buss is latched into the eight bit latch contained on the display processor board when its I/O strobe is addressed. In order to get this latched information onto the internal display data buss, the display processor must be forced to tri-state all of its data/address bus drivers and control line drivers. When this is accomplished, the output enable of the input latch (U6 pin 1) can be pulled low which will cause the outputs of U6 to drive the internal data/address bus with the bit pattern stored there by the instrument processor. The above can be accomplished by making the following connections on the display processor:

CONNECT LRESET (U9 pin 3) to GROUND

CONNECT EA (T.P. 8) to +12 v (T.P. 13)

CONNECT LREAD (U6 pin 1) to GROUND

The following signatures may be obtained by probing any point on the display connected to that node:

SIGNAL NAME	LOCATION	SIGNATURE
INST DB0	J2-3	H186
INST DB1	J2-4	CFPH
INST DB2	J2-5	H077
INST DB3	J2-6	0942
INST DB4	J2-7	CC29
INST DB5	J2-8	63CP
INST DB6	J2-9	F77H
INST DB7	J2-10	2757
INST ADR0	J2-23	AUCU
INST ADR1	J2-24	U154
INST ADR2	J2-25	012F
INST ADR3	J2-26	8U24
INST ADR4	J2-27	7UUF
INST SIOA	J2-49	1714
D0	U6 pin 12	5056
D1	U6 pin 15	A239
D2	U6 pin 9	46P7
D3	U6 pin 6	8U5C
D4	U6 pin 16	1F22
D5	U6 pin 5	73C7
D6	U6 pin 19	P76U
D7	U6 pin 2	FF4C
LEN 5	U10 pin 10	2563
LEN 7	U10 pin 7	52CA

In order to check the latched information in the annunciator latches (U5 & U7) the jumpers added on the display must be removed. TURN OFF the instrument when removing these jumpers or be sure to remove the jumper between +12 V and EA first. After removing the three jumpers the following signatures may be obtained by probing the outputs of the annunciator latches:

SIGNAL NAME	LOCATION	SIGNATURE
CF	U5 pin 2	A18U
DELTA F	U5 pin 5	9A09
START	U5 pin 7	PH05
CW	U5 pin 10	031F
UNLVLD	U5 pin 12	HU2P
FAULT	U5 pin 15	508P
OVERMOD	U7 pin 10	H05A
OVEN	U7 pin 12	A0C4
EXT REF	U7 pin 15	4169
FAULT	U7 pin 2	15HH
SRQ	U7 pin 5	U2AH
REMOTE	U7 pin 7	3F4F

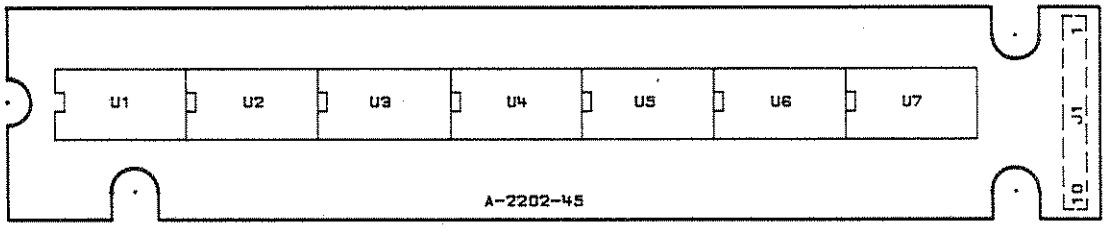


Figure 8-505. A1 Alpha Display,
Component Location Diagram
8-285/8-286

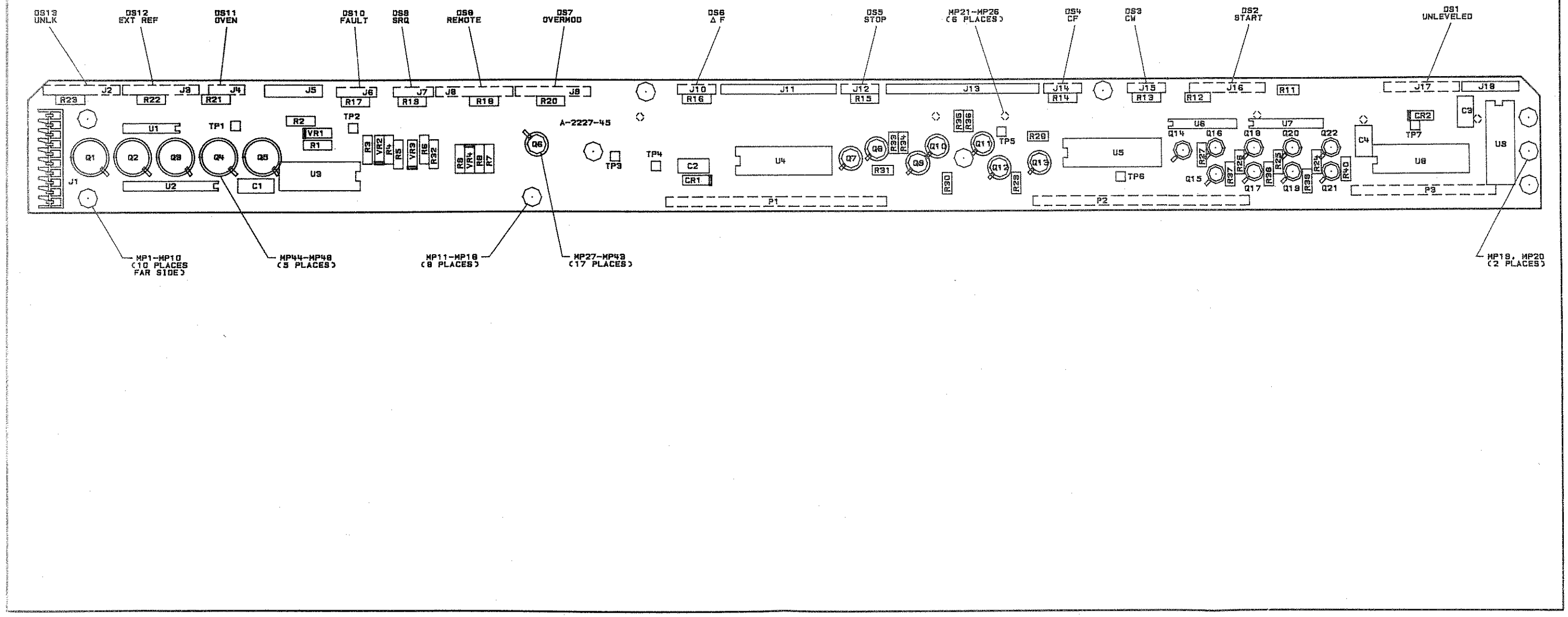
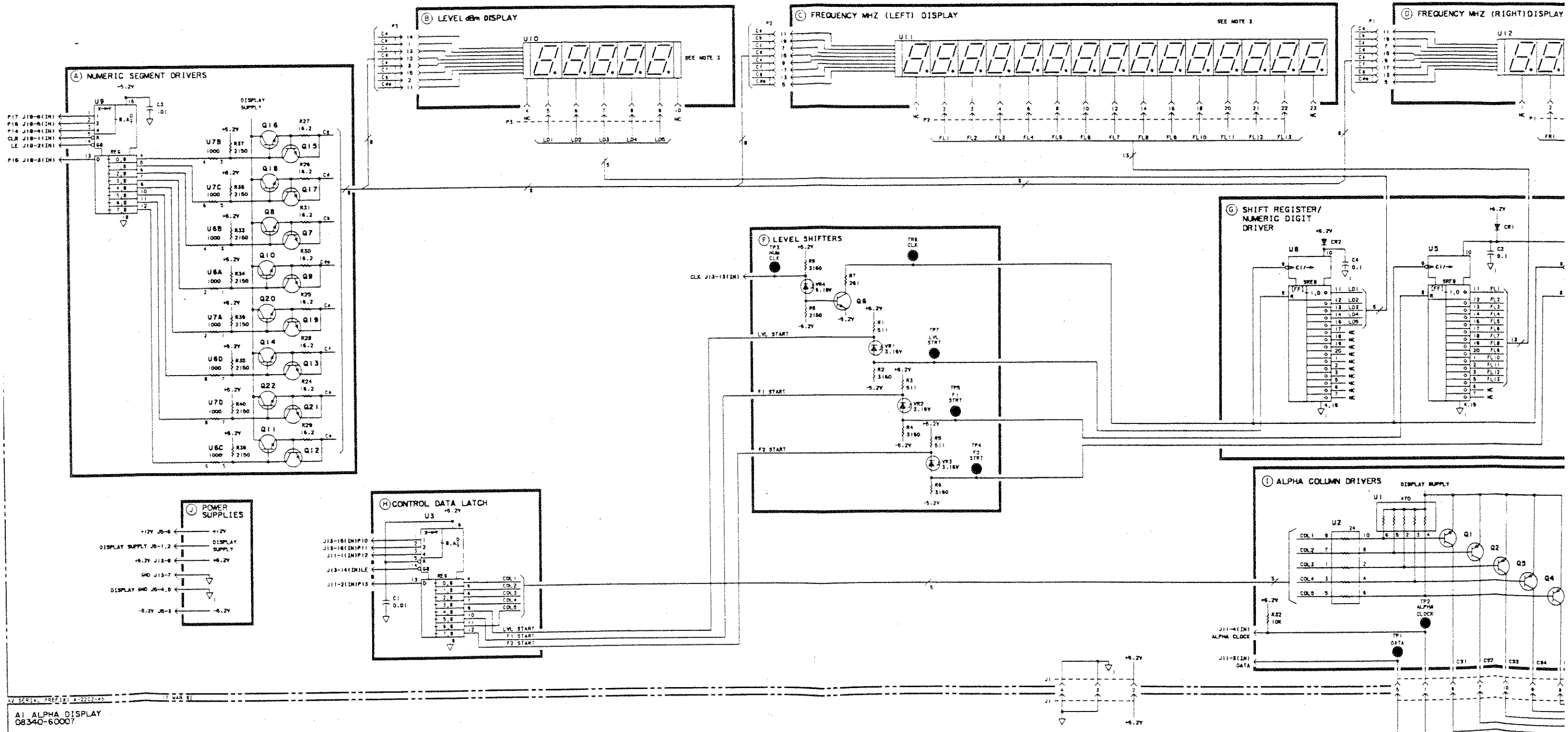


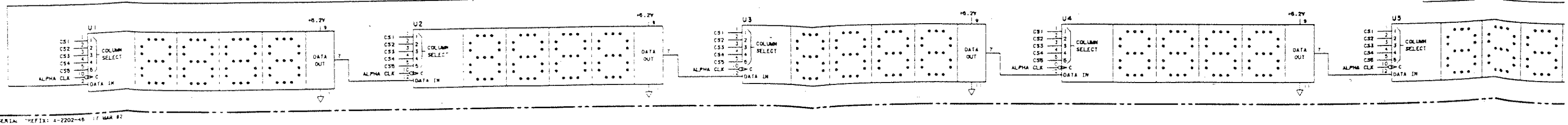
Figure 8-506. A2 Display Driver,
Component Location Diagram

A2 DISPLAY DRIVER
08340-60009

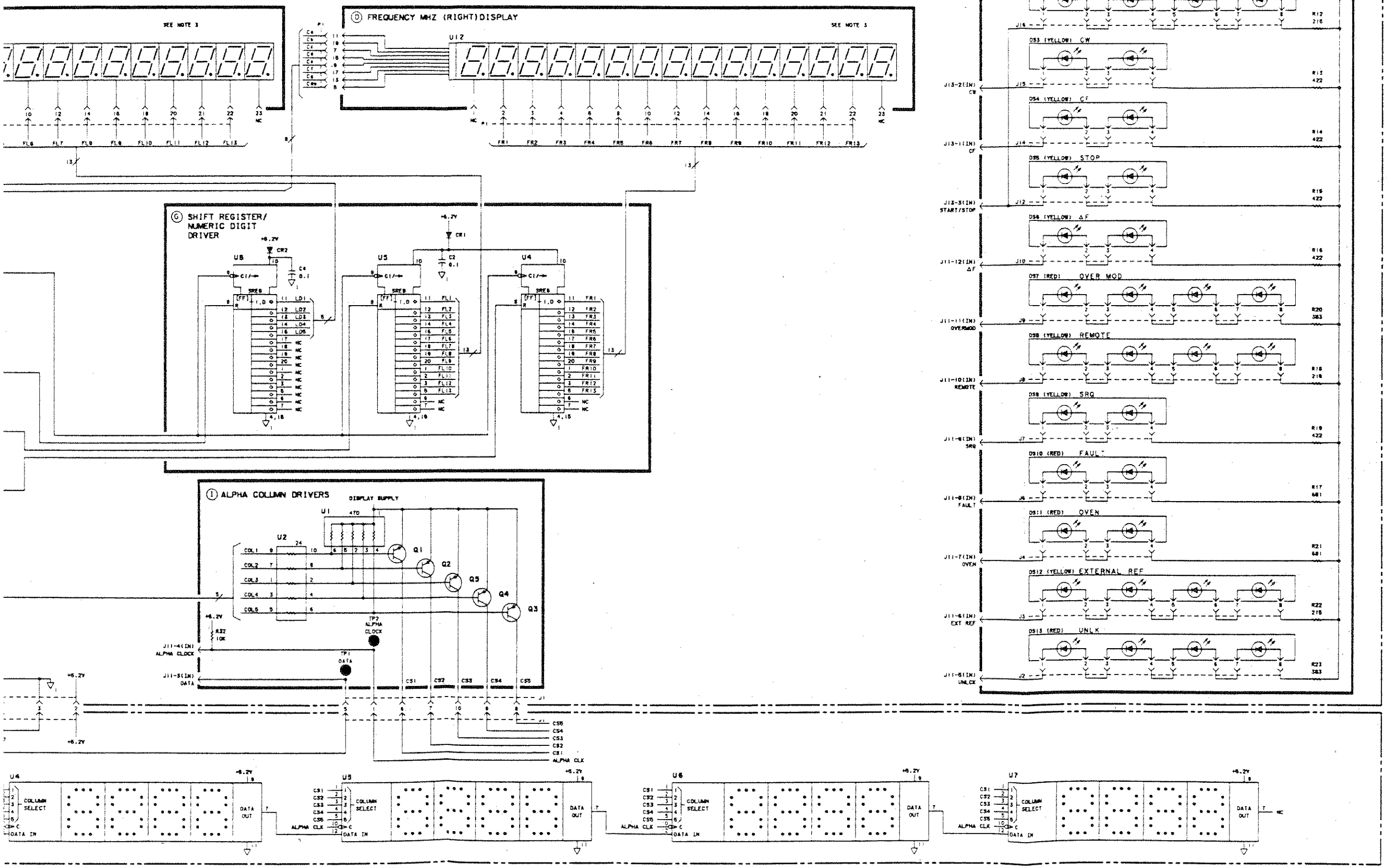


A2 SERIAL PREFIX: A-2202-46 17 MAR 82

A1 ALPHA DISPLAY
08340-60007



A1 SERIAL PREFIX: A-2202-46 17 MAR 82



1. REFER TO FIGURE 8-4 FOR DETAILED SCHEMATIC DIAGRAM SYMBOLOGY NOTES.
2. RESISTANCE VALUES SHOWN ARE IN OHMS, CAPACITANCE IN MICROFARADS, AND INDUCTANCE IN MICROHENRIES UNLESS OTHERWISE NOTED.
3. U10,U11 AND U12 ARE MATCHED FOR SIMILAR LUMINOUS INTENSITY.

Figure 8-509. A1 Alpha Display and A2 Display Driver, Schematic Diagram

NOTES

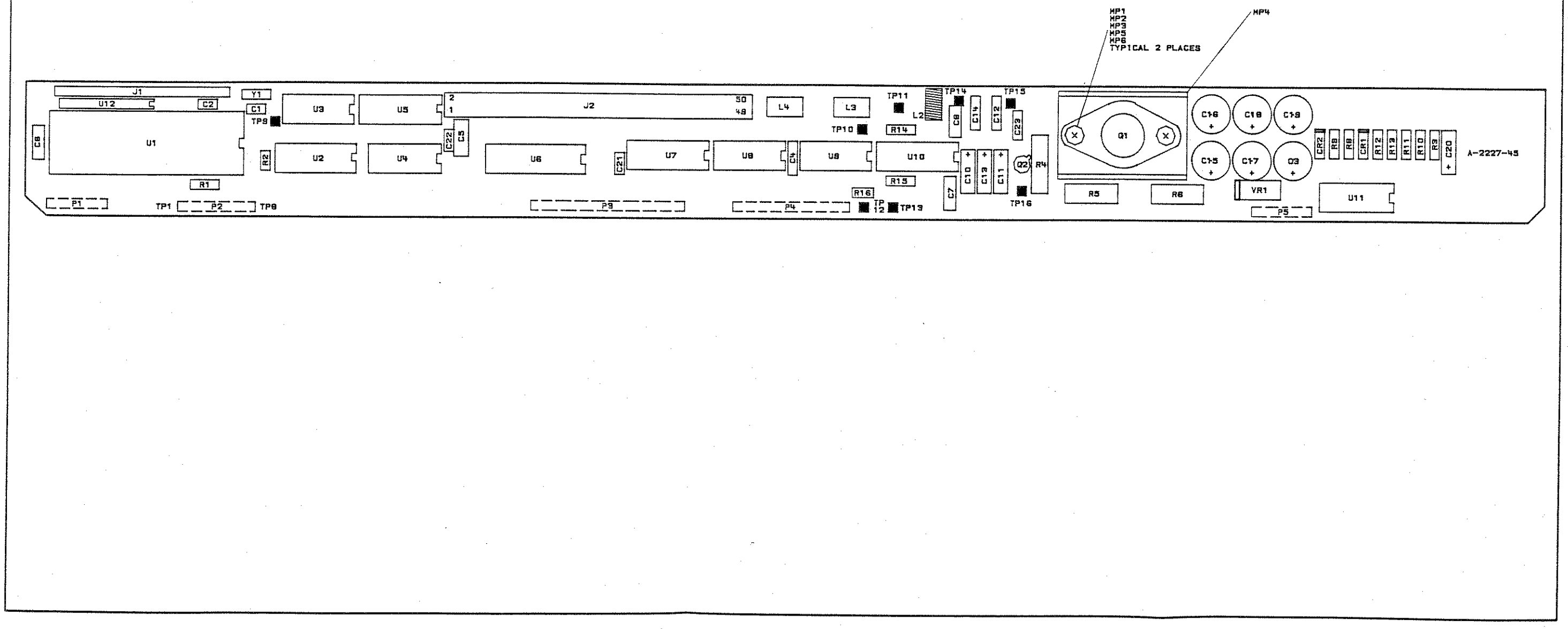
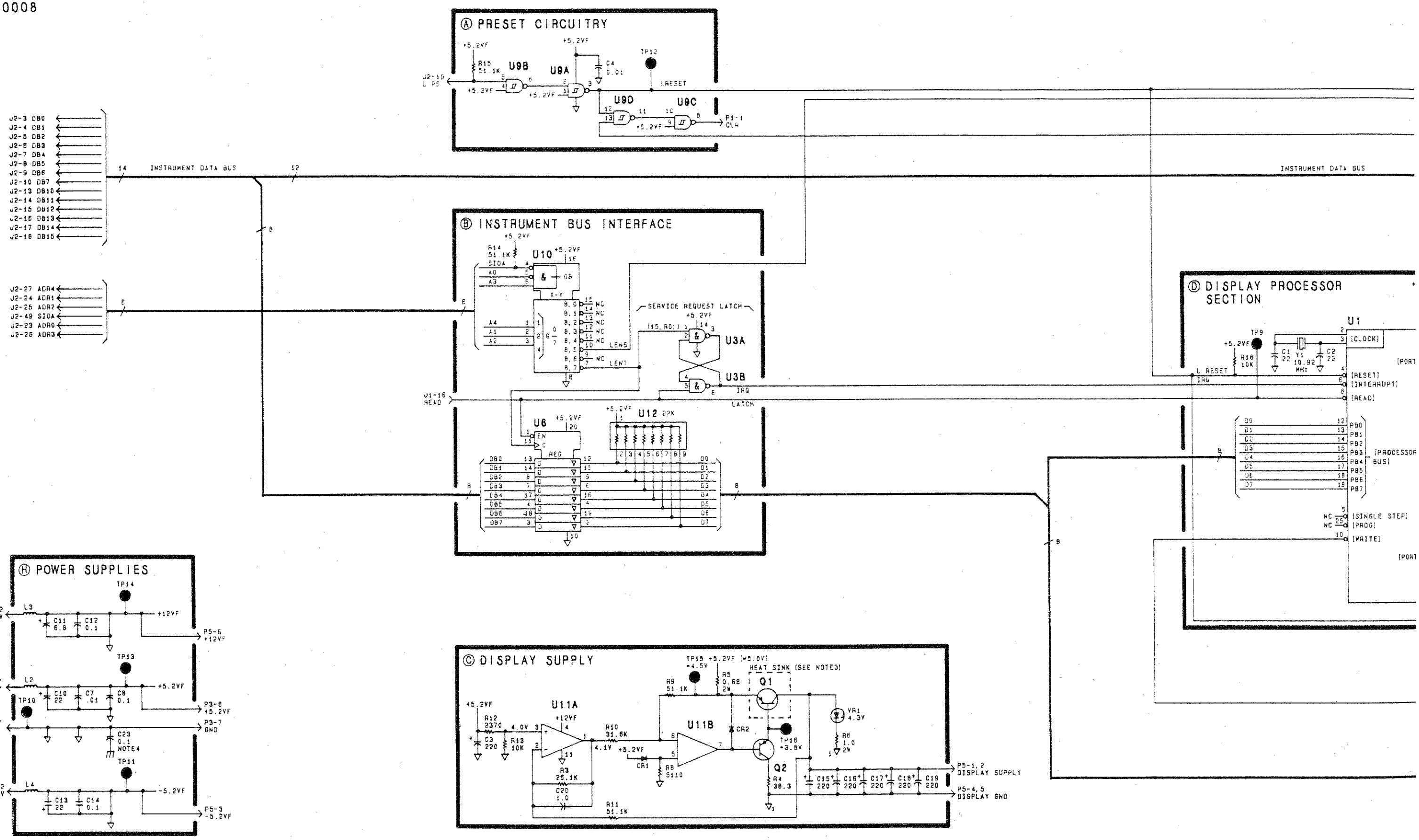


Figure 8-513. A3 Display Processor,
Component Location Diagram

3 DISPLAY PROCESSOR/CURRENT SOURCE
083540-60008



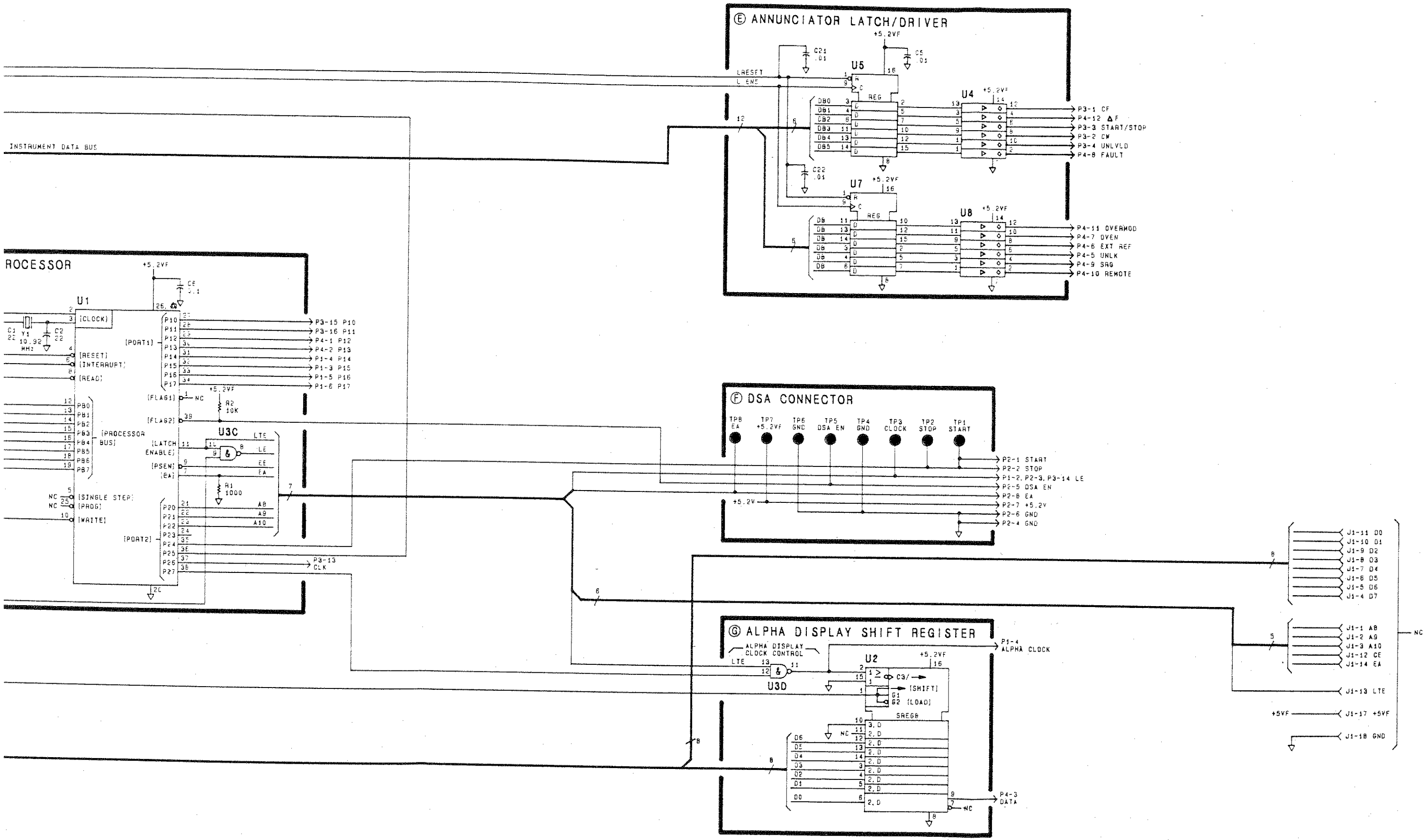


Figure 8-515. A3 Display Processor, Schematic Diagram

A5 KEYBOARD AND A7 LOWER KEYBOARD, CIRCUIT DESCRIPTION

The keyboard section includes the A5 Keyboard Assembly, the A7 Lower Keyboard Assembly, and the A6 Keyboard Interface Assembly.

Annunciators A (A5 and A7)

The annunciator LED's are driven from latches on the A6 board. The anode of each annunciator is tied to +5V through a resistor. The annunciators are turned ON by a LOW from the A6 latches.

Main Keyboard A5 B
Lower Keyboard A7 B

The two keyboards contain 58 keys which have a multi-finger contact structure. Each key shorts one column line and one row line to digital ground.

There is not a general patern followed for the encoding of the rows and columns, however, it may be necessary to determine from the schematic diagram what row and column each key translates to during trouble shooting.

A6 KEYBOARD INTERFACE, CIRCUIT DESCRIPTION

Keyboard Encoder/Data Buffer A

Eight line to three line priority encoders (U1 and U10) are used to encode the row and column information. When a key is pressed one row line and one column line is grounded by the key. The row and column is encoded and is presented in LOW TRUE binary form at the outputs (U1 and U10 pins 9, 7 and 6). This information is immediately available at the inputs of U11 the 74LS240 inverting output buffer which converts the above six bits to HIGH TRUE signals. Table 8-526A shows the Keyboard Encoder Logic.

TABLE 8-526A. Keyboard Encoder Logic

Column or Row Selected Low	Output of U10 or U11 Pin 9	7	6
0	1	1	1
1	0	1	1
2	1	0	1
3	0	0	1
4	1	1	0
5	0	1	0
6	1	0	0
7	0	0	0

If more than one key is pressed, the priority encoder only encodes the lowest column and row number.

The encoders are enabled by a latched control bit (1 written to bit 7 of address 6,R1:). This control line is used to lockout the keyboard.

When any key is pressed the encoders generate a LOW TRUE key-down (U10 pin 14) signal which starts the rest of the key encoding operations.

Key Up Timer (Debounce) B

The key released timing function prevents key bounce from causing multiple keydown interrupts to the main processor. This is accomplished by disabling the key down circuitry as doon as a valid key down has been detected and not re-enabling it until all keys have been up continously for 100 mS.

As soon as a key is depressed, the REPEAT DISABLE signal (U14B pin 4) goes HIGH when the KEYBOARD LOCKOUT signal (U14B pin 6) is LOW. This REPEAT DISABLE SIGNAL is inverted twice (U8 pin 3-4, 9-8) and appears at the input of a NOR gate (U14D pin 12). The other input to this NOR gate (U14D pin 11) is connected to the Q output of the keyup one shot (U9B pin 5) which will go HIGH for 100 mS after the positive transition of the Key Down Start signal (U9B pin 10). The output of the above NOR gate (U14C pin 13) goes LOW and is inverted (U14C pin 9). The output of the inverter (U14C pin 10) causes the reset line of a D flip-flop (U4A pin 1) tof go HIGH which enables this flip-flop. The HI KEY DN SRQ line is connected to the clock line (U4A pin 3) so as soon as a valid key down has been detected, the flip-flop will be set. The Q-bar output (U4A pin 6) goes directly to the enable of the key down one shot (U20B pin 10 in Block C) which prevents detecting any further key clowures until this enable goes HIGH.

When the key is released the LOW KEY DOWN line goes HIGH which fires a one shot (U9B pin 10) for 100 mS which continues to disable the key down circuitry until it has timed out.

The 0.01 uF capacitor C23 connected to the output of U8B pin 4 was added to prevent a possible race condition. The input to U14D pin 12 must remain HIGH until the one shot output going to U14D pin 11 is HIGH and stable. Since the one shot is fired by the same signal that goes into U14D pin 12, some means of delay had to be implemented. Both digital and analog delay are used to prevent a parametric change from causing a race condition.

At the end of 100 mS, the one shot output (U9B pin 5) goes LOW

which causes the key down disable flip-flop to be cleared (U4A pin 1) which in turn re-enables the key down flip-flop (U20B pin 10 in Block C).

Key Down Timer C

The LOW KEY DOWN signal fires a non-retriggerable one shot (U20 pin 9) which is set for approx. 20 mS. pulses. The Q-bar output (U20 pin 12) goes low for 20 mS and on its rising edge it clocks a D-flipflop (U19 pin 11) whose D input (U19 pin 12) is connected to the LOW KEY DOWN signal. If a key is still down at this momment, the D-flipflop is reset indicating that a valid key down has been detected.

When a valid key down is detected, the Q-bar output (U19B pin 8) goes high and this is the HI KEY DOWN SRQ.

Repeat Function Circuits D

The repeat key function consists of two timing circuits. The first is a 500mS (U9A) timer which is triggered by the Q output of the key down flip-flop (U19B pin 9 Block C) when a valik key down has been detected. After 500 mS the rising edge of the Q-bar output of this one shot (U9A pin 4) clocks a D flip-flop (U4B pin 11). The D input (U4B pin 12) is connected to the LOW KEY DOWN line from the encoders (U10 pin 14 in BLOCK A). If a key is still down 500 mS after a valid key has been detected this flip-flop U4B will be reset activating the repeat function. The Q-bar output of this flip-flop (U4B pin 8) goes high which releases the reset of the second timer (U5A pin 4) and allows it to generate high going pulses at a 5 Hz rate.

The second timer (U5A) is a 555 timer. The timing components (R1,R2,CR1,C8) were selected so that high going pulses with a very low duty cycle would be generated. The high going output (U5 pin 3) of this timer goes thru an inverter (U14A pin 3 to 1) and becomes LOW REPEAT to the RESET of the key-down SRQ flip flop (U19B pin 13) which has the same effect as pressing the key again. The duration of the reset pulse to this flip flop (U19B) must be shorter than the fastest time that the main processor can get around to servicing the key-down interrupt or else another key-down SRQ cycle will be immediately started.

Annunciator Latches E

Four 8 bit D-latches (U6, U7, U16 & U17) store LED & control information. 29 bits control all of the various LEDs on the front panel. One bit is an INST PR LOCKOUT (U16 pin 2) which is Anded with the input from the hardware instrument preset signal (Block J). One bit is the lockout for the rest of the keyboard

(KEYBOARD LOCKOUT U6 pin 2) which prevents any keyboard entries. The last bit (U17 pin 9) is unused.

The same bit (U6 pin 19) that turns on the enabled LED (ENTRY ON) also enables the RPG (U19 pin 2 Block H). U19 pin 2 is the D input.

The green SWEEP LED is driven by an inverter (U2C pin 8, LOW = LED ON) which is controlled by a nand gate. This NAND gate forces the LED to be ON when the Instrument Preset signal (U2A pin 3 Block J) is LOW and when LSPLP (Low Sweep LED) is LOW.

Address Decoder F

A 74LS138 (U15) is used to decode four strobes from the five Address lines and the I/O strobe (SIOB). Channel 6 subchannel 0 and 1 (U15 pin 11&10) are used to clock the LED and control input D-latches (U6,U7,U16,U17 Block E). Channel 6 sub-chan 2 (U15 pin 9) resets the Key down and RPG service request circuitry. The last stobe (U15 pin 7) is a read strobe and enables the coded key information, the RPG count information and the two bits which indicate which circuit requested service onto the buss to be read by the processor.

RPG Counters Data Buffers G

The rotary pulse generator (RPG 1) generates two pulses which are 90 degrees out of phase with each other when the knob is turned.

Two four bit up/down counters (U13 & U18) count up or down depending on the direction in which the RPG is turned. The two signals from the RPG (which are 90 degrees out of phase) are connected to the up/down input (U13 & U18 pin 1) and to the clock input (U13 & U18 pin 2). If the clock line goes high while the up/down line is still low, the counters count down. On the other hand if the RPG is turned in the opposite direction, the up/down line will be HIGH when the clock line goes HIGH and the counters will count up. When the counter counts down below 0, the output is set to all ones and counted down from there.
The outputs of the up/down counters (U13 & U18 pins 13 thru 16) are always present at the inputs to the noninverting buss driver from which the main processor reads present count.

The up/down counters are cleared by the processor (U13 & U18 pin 8) after the information is read which readies them for the next count period.

A 0.01 uF cap is connected to the CLK line and the up/down line (C13 and C14) from the RPG (U8 pins 11 & 13) to prevent static discharges from clocking the up/down counters.

RPG Count/Window Timer H

The CLK line that goes to the up/down counters from the RPG is connected to the clock of a 70 mS one shot (U20A pin 2). The very first pulse on the RPG clock line fires the one shot. At the end of 70 mS, the one shot output (U20A pin 4) clocks the clock of a D flip flop (U19A pin 3). If the RPG is enabled, the D input to this flip flop (U19A pin 2) will be LOW and the Q-bar output (U19A pin 6) will go high causing the LSRQ (Block I) line to go low indicating a service request to the processor. The Q-bar output (U19A pin 6) also goes to the input of the inverting buss buffer (U11 pin 17 in Block A) the inverted output of which is read by the processor during the service request routine. A LOW on this line indicates that it was the RPG which needed service.

The RPG SRQ line also goes to the disable count input of the up/down counters (U13 & U18 pin 7 Block G) which disables any further counting until the processor has serviced the RPG service request.

After the main processor has read the information from the up/down counters, a reset strobe is generated (U15 pin 9 address 6,R2: block F) by the processor which sets the RPG SRQ flip flop and clears the up/down counters and prepares the whole circuit for another cycle.

SRQ Buffer I

The HI KEY DN SRQ signal is Nor'ed (U3 pin 3) with the HI TRUE RPG SRQ (U3 pin 2) signal to generate LSRQ (U3 pin 1) to the instrument processor.

The HI KEY ON-SRQ signal is also present at an input to

U11 pin 2 which contains the encoded key information. This bit, when read by the processor during a SRQ service routine, indicates that it was a key-down that generated the service request. U11 inverts this signal so the processor sees a LOW TRUE signal.

Once the instrument processor has read the encoded information, the processor generates a strobe (Block F U15 pin 9 address 6,R2:) which sets the SRQ flipflop (Block C U19B pin 10) indicating that key information has been read by the processor and prepares the key down circuitry for the next key-down signal.

A keyboard lockout signal (Block E U6 pin 2) is inverted (Block C U8C pin 5 to 6) and if it is LOW it resets the keydown one shot

and prevents this one shot from ever firing.

Power Switch And Stand-By LED

During standby operation, the power switch grounds the LSBY line which activates the fan relay and signals the power supplies to turn off.

The standby LED is connected to the +22 volt supply thru a current limiting resistor. The power switch grounds the cathode of this LED during standby thus turning on the LED.

TROUBLESHOOTING USING THE INSTRUMENT DSA ROUTINE

A limited amount of DSA is available on the keyboard controller. All of the latched LED Bits and Control Bits as well as the Strobes can be tested for correct operation by using this DSA routine and a Signature Analyzer.

This DSA mode can be activated by grounding the STS TP on the Processor board and then turning the instrument off and then on again. The Signature Analyzer must be connected as follows:

START connected to TP t1 on the memory board
trigger on the rising edge

STOP connected to TP t2 on the memory board
trigger on the rising edge

CLOCK connected to TP IOSB on the processor board
trigger on the rising edge

GRND connected to chassis ground or ground pin

The following signatures may be verified by probing any point on the keyboard controller that is connected to that node with the Signature Analyzer:

SIGNAL NAME	LOCATION	SIGNATURE
INST DB0	P7-3	H186
INST DB1	P7-4	CFPH
INST DB2	P7-5	H077
INST DB3	P7-6	0942
INST DB4	P7-7	CC29
INST DB5	P7-8	63CP
INST DB6	P7-9	F77H
INST DB7	P7-10	2757

INST DB8	P7-11	P702
INST DB9	P7-12	67A8
INST DB10	P7-13	FU51
INST DB11	P7-14	9PA2
INST DB12	P7-15	3H44
INST DB13	P7-16	37FH
INST DB14	P7-17	CF15
INST DB15	P7-18	H186
INST ADR0	P7-23	AUCU
INST ADR1	P7-24	U154
INST ADR2	P7-25	012F
INST ADR3	P7-26	8U24
INST ADR4	P7-27	7UUF
INST SIOB	P7-47	3704
LEN 4	U15 pin 11	P769
LEN 5	U15 pin 10	U034
LEN 6	U15 pin 9	FAFP
LEN 7	U15 pin 7	2019*
MRKR SWP	U6 pin 12	8H01
M1	U6 pin 9	2156
M2	U6 pin 15	79U9
M3	U6 pin 6	F8A6
M4	U6 pin 16	AA19
M5	U6 pin 5	H973
ENTRY ON	U6 pin 19	AP4U
KEYBOARD LOCKOUT	U6 pin 2	7C63
ALTN	U7 pin 19	FH92
EXT	U7 pin 2	A070
SINGLE	U7 pin 16	5F49
MAN	U7 pin 5	C892
FREE	U7 pin 15	7124
LINE	U7 pin 6	F5C5
CONT	U7 pin 12	C03U
DELTA MRKR	U7 pin 9	5C2A
PEAK	U16 pin 12	CC23
XTAL	U16 pin 9	0UFP
AMPTD MRKR	U16 pin 15	6614
PWR SWP	U16 pin 6	C5A1
INT	U16 pin 16	12FC
RF	U16 pin 5	10PH
EXT	U16 pin 19	H7A5
INST PR LOCKOUT	U16 pin 2	20CH
AM	U17 pin 19	38U3
SLOPE	U17 pin 2	086U
PULSE	U17 pin 16	P6A0
INST CK I	U17 pin 5	FH41
INST CK II	U17 pin 15	9A82
FM	U17 pin 6	CAU3
SHIFT	U17 pin 12	0F6P
UNUSED	U17 pin 9	6155

* THIS I/O STROBE IS USED FOR ONE OF THE DSA FUNCTIONS AND THEREFORE DOES NOT HAVE A UNIQUE SIGNATURE (SAME AS +5 V). TO CHECK THIS STROBE IF IT IS SUSPECTED TO BE SHORTED HIGH, SEE THE MAIN IO BUSS DSA TEST PROCEDURE IN THE PROCESSOR SECTION TITLED "ADDRESSING EXERCISE".

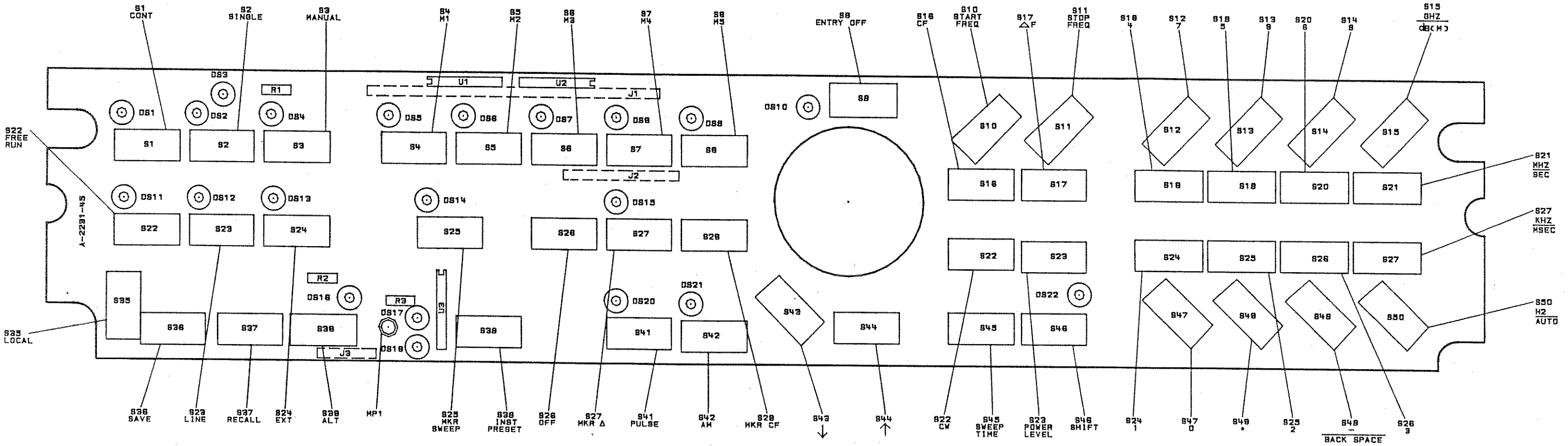


Figure 8-520. A5 Keyboard, Component Location Diagram

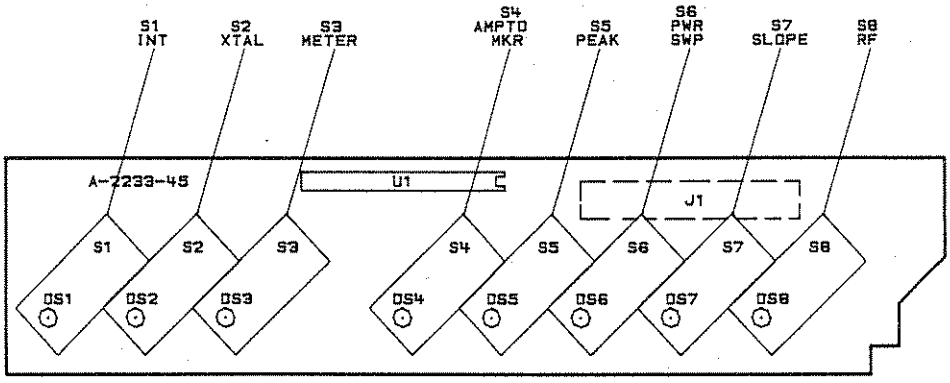
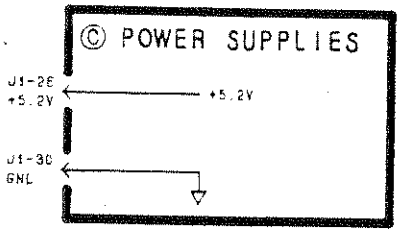
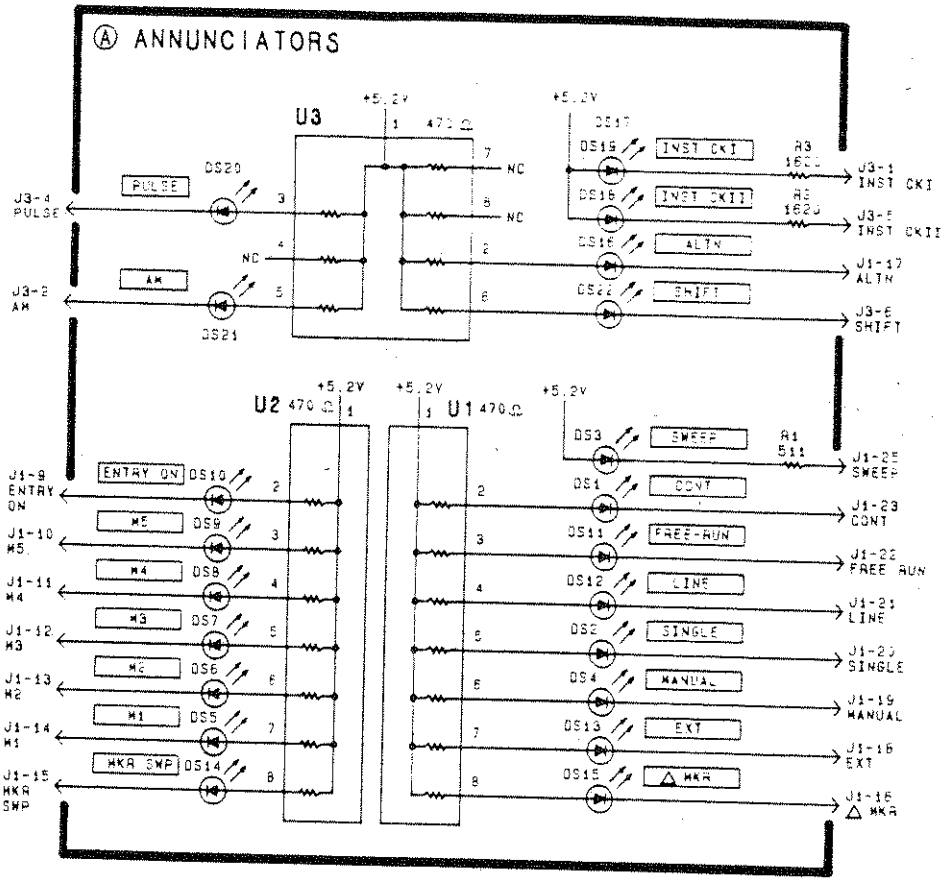


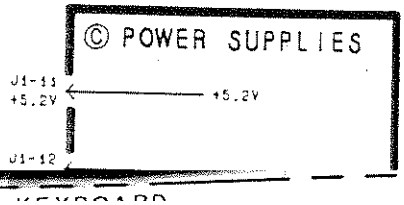
Figure 8-521. A7 Lower Keyboard, Component Location Diagram

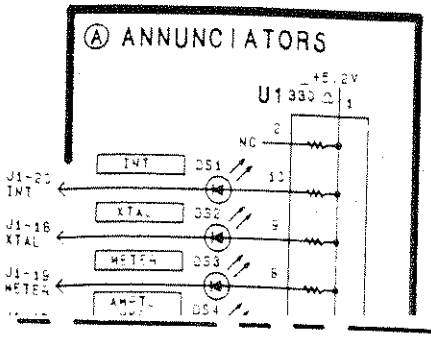
KEYBOARD
08340-60010

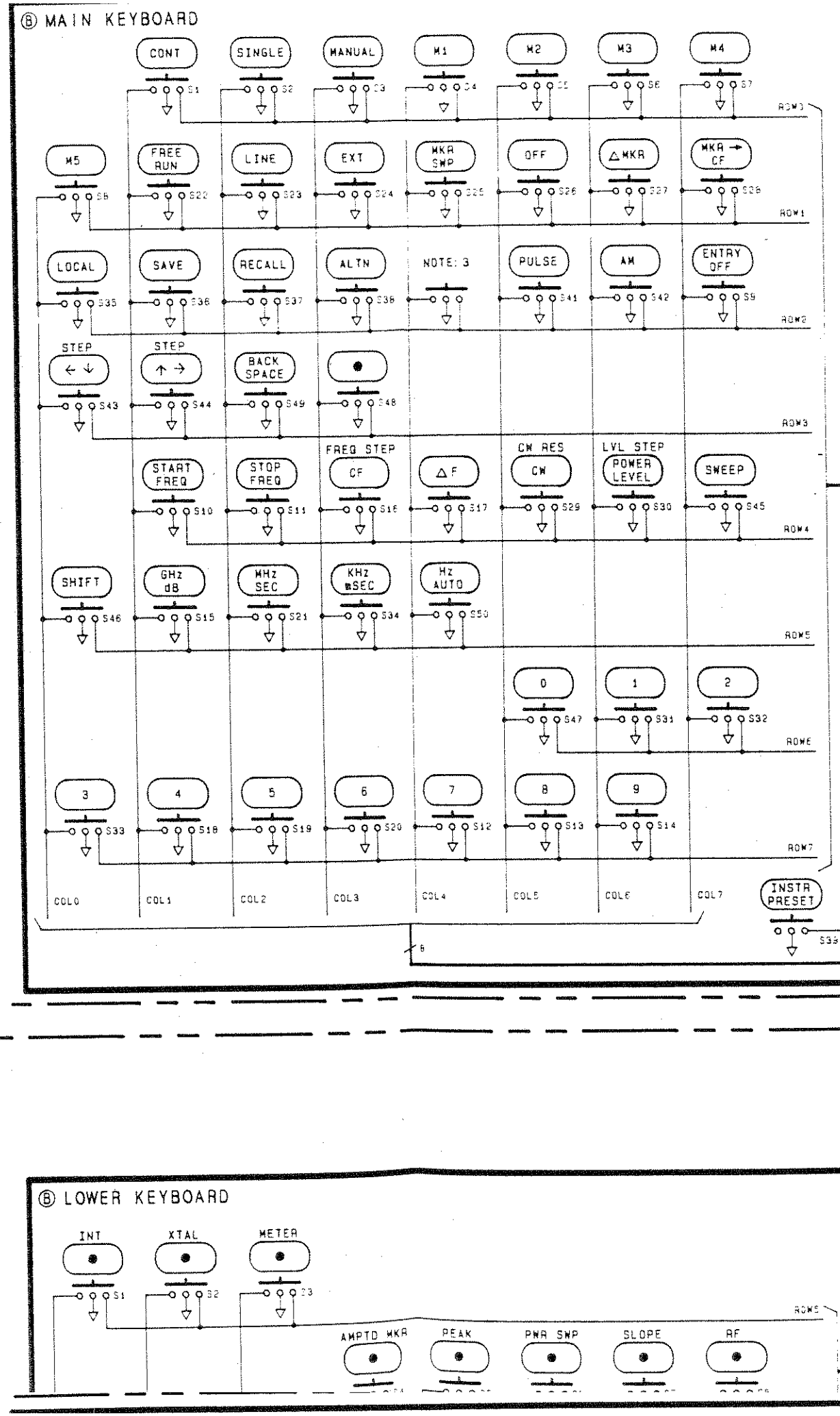


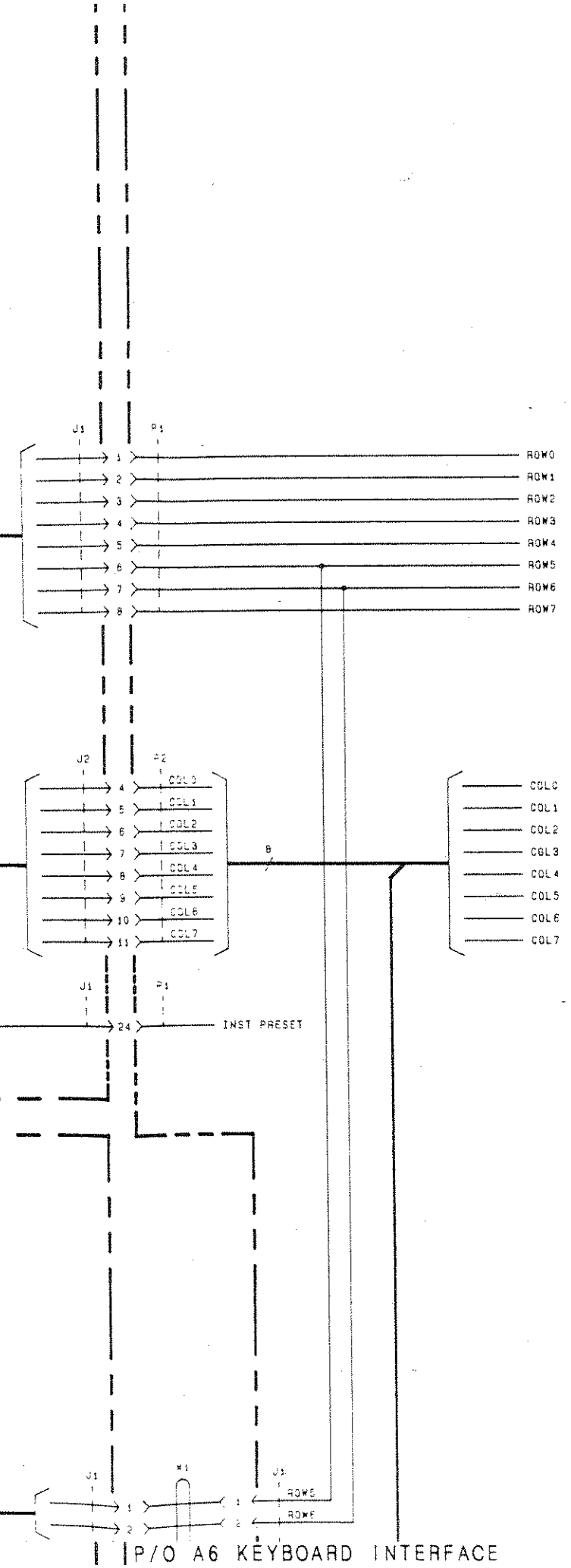


LOWER KEYBOARD
08340-60012

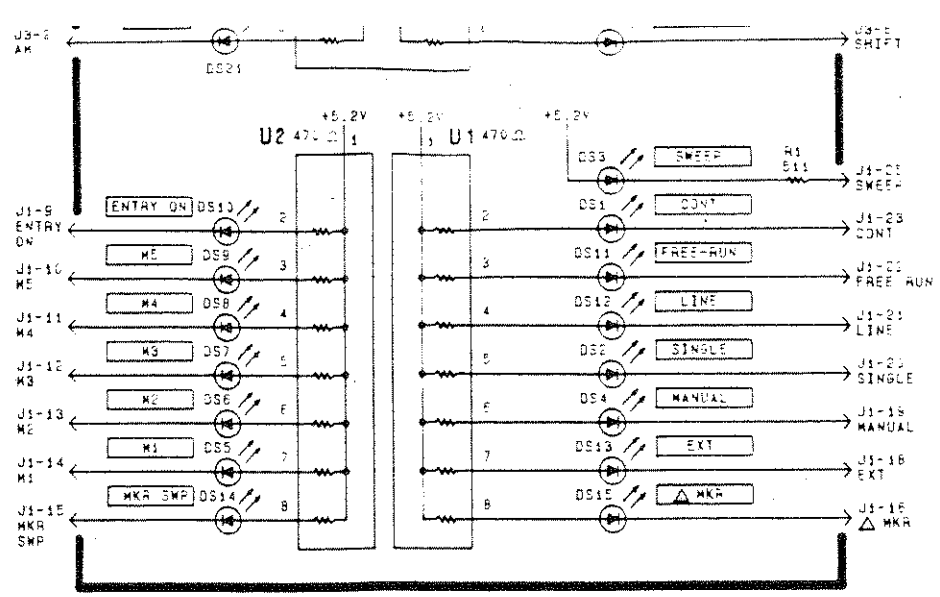


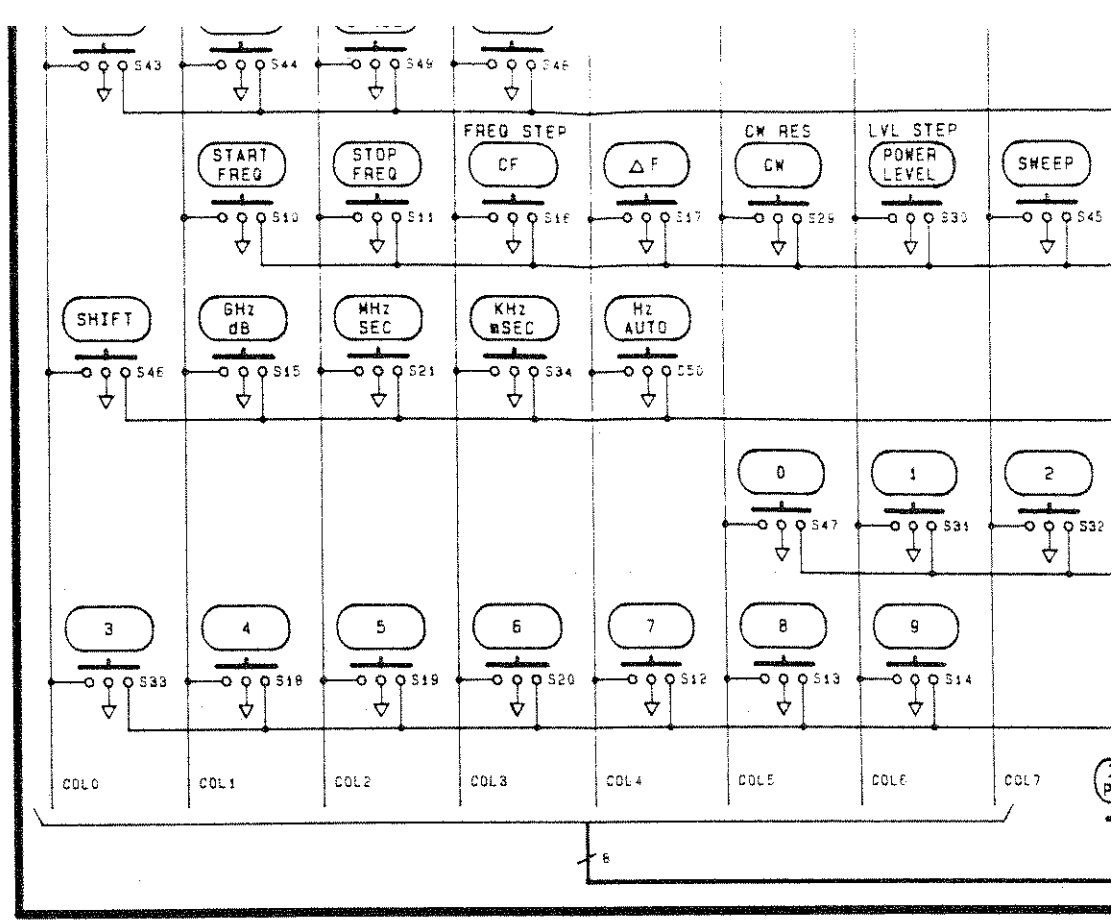




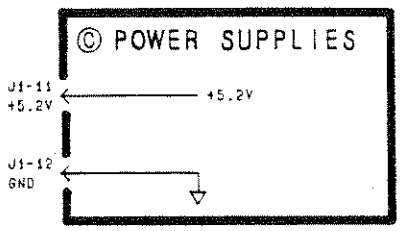


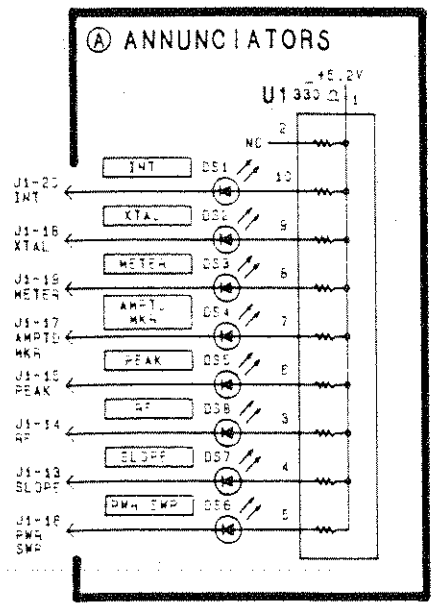
1. REFER TO FIGURE 8-4 FOR DETAILED SCHEMATIC DIAGRAM NOTES.
2. RESISTANCE VALUES ARE IN OHMS, CAPACITANCE IN MICROFARADS, AND INDUCTANCE IN MICROHENRIES UNLESS OTHERWISE NOTED.
3. RESERVED FOR FUTURE USE.

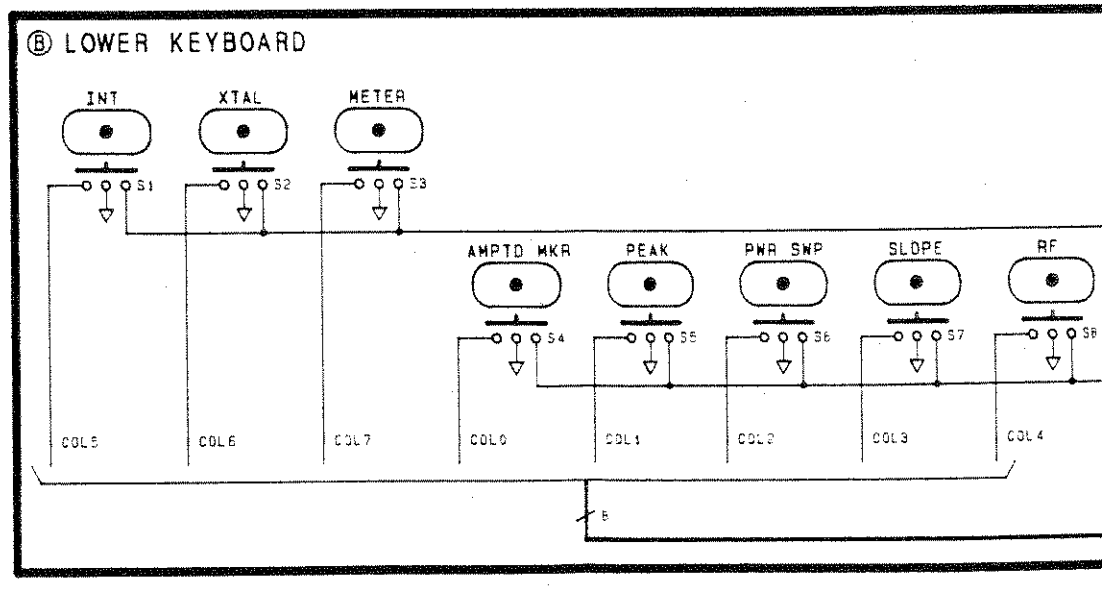




A7 LOWER KEYBOARD
08340-60012







A5 SERIAL PREFIX: A-2231-45 A7 SERIAL PREFIX: A-2233-45 OPTII FILE NO. DB1

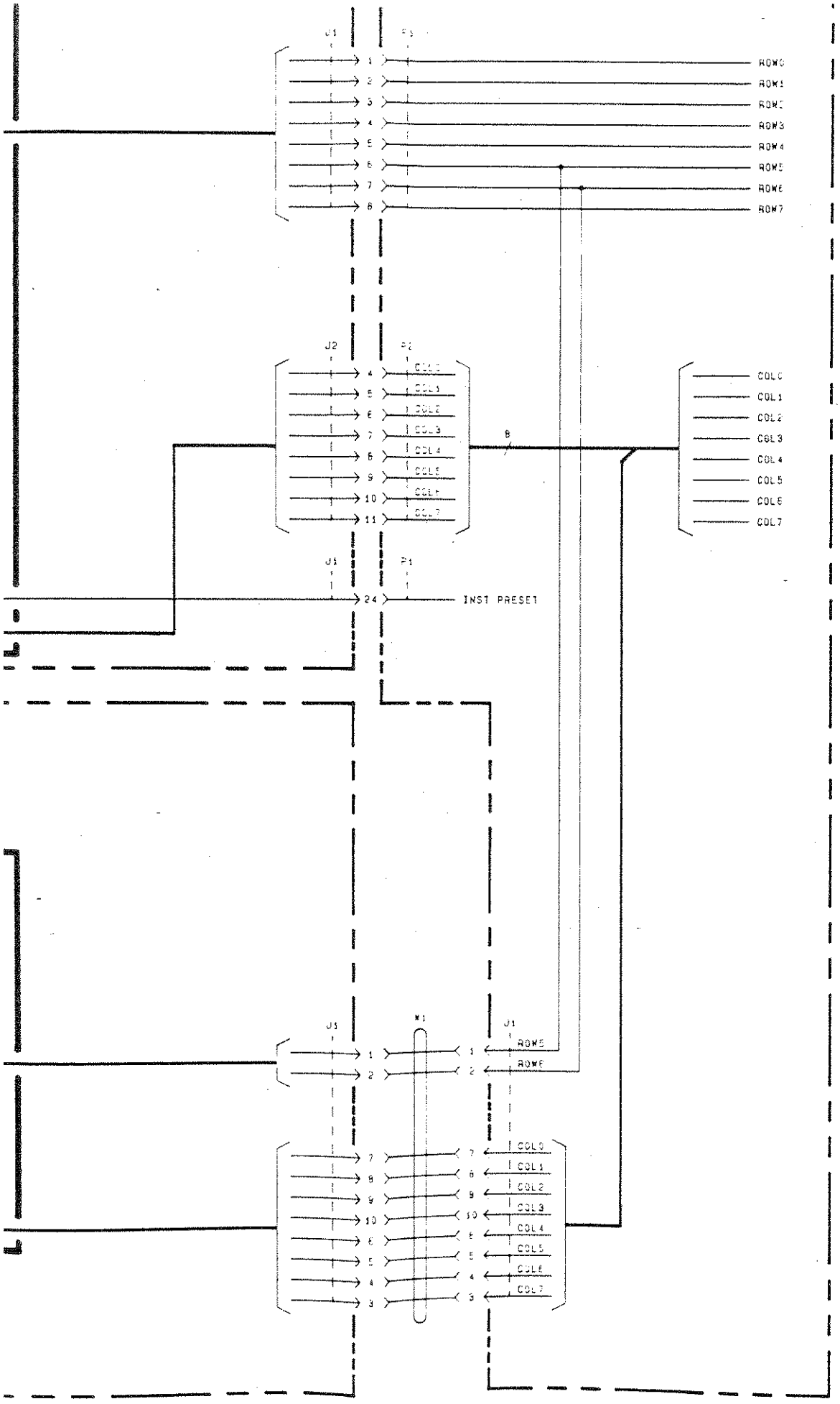


Figure 8-524. A5 Keyboard and A7 Lower Keyboard, Schematic Diagr

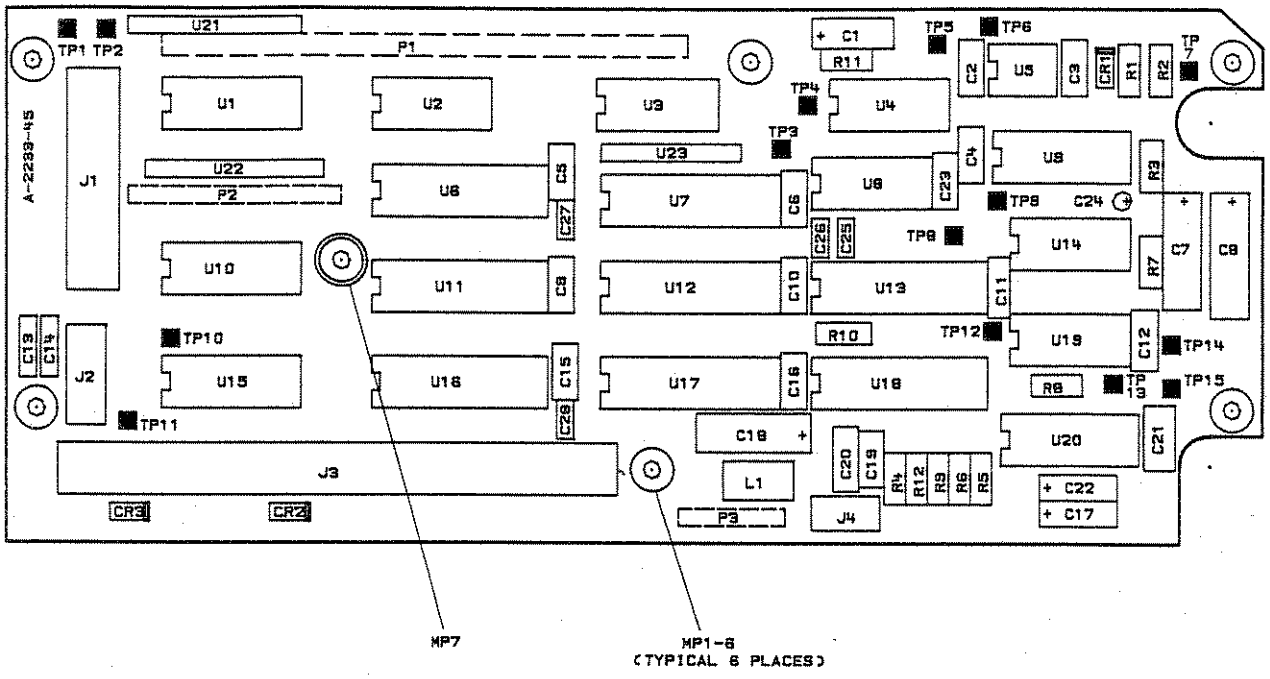


Figure 8-528. A6 Keyboard Interface, Component Location Diagram

J3-3 (I/O) D00
J3-4 (I/O) D01
J3-5 (I/O) D02
J3-6 (I/O) D03
J3-7 (I/O) D04
J3-8 (I/O) D05
J3-9 (I/O) D06
J3-10 (I/O) D07
J3-11 (I/O) D08
J3-12 (I/O) D09
J3-13 (I/O) D010
J3-14 (I/O) D011
J3-15 (I/O) D012
J3-16 (I/O) D013
J3-17 (I/O) D014
J3-18 (I/O) D015

+22V
R12 4640
R4 4640
J4
STANDBY
LSBY
N.C.
ON
J4

A KEYBOARD ENCODER/DATA BUFFER

U22 OK +5.2V
U10 +5.2V
+5.2V BUS
U11
C9 0.1
P2-4,P5-7 (IN) COL0
P2-5,P5-8 (IN) COL1
P2-6,P5-9 (IN) COL2
P2-7,P5-10 (IN) COL3
P2-8,P5-6 (IN) COL4
P2-9,P5-5 (IN) COL5
P2-10,P5-4 (IN) COL6
P2-11,P5-3 (IN) COL7
CR2
J3-28 L STEPUP
CR3
U21 OK +5.2V
U1 +5.2V
P1-1 (IN) ROW0
P1-2 (IN) ROW1
P1-3 (IN) ROW2
P1-4 (IN) ROW3
P1-5 (IN) ROW4
P1-6,J1-1 (IN) ROW5
P1-7,J1-2 (IN) ROW6
P1-8 (IN) ROW7
LOW KEY DOWN

B KEY UP TIMER (DEBOUNCE)

+5.2VF
R7 34.8K
U9B
C24 2.2
(TIMING)
LOW KEY DOWN
+5.2VF
R
U14B U8B U8D
C23 0.01

C KEY DOWN TIMER

+5.2V
R5 28.7
C17 .10
TP3
KEYBOARD LOCKOUT
U8C
LOW KEY DOWN

D ADDRESS DECODER

+5.2V
U15
J3-47 SCIB
J3-25 A2
J3-26 A3
J3-23 A0
J3-24 A1
J3-27 A4
J3-21 GND
IN 4/6 P0

G RPG COUNTERS/DATA BUFFERS

U18 +5.2V
+5.2V BUS
U12
C10 0.1
U13 +5.2V
C11 .01
U8E
U8F
C25 0.01
C26 0.01
TP2

H RPG COUNT WINDOW T

(RPG COUNT WINDOW TIMING CIRCUIT =/-2mS)
+5.2V
R8 10K
U19A
C22 2.2

X POWER SUPPLIES

J3-50 +22V
J3-2 +12V
TP6 +5.2VF
J3-34,36,37, 51,52 +5.2V
C18 22
C19 0.1
C20 0.01
J3-1,2,29,48, 46,50 GND PT
TP4 GND
J3-42 -5V
J3-53,55 +5.2V BUS
J3-38,39,40

FRONT PANEL CHASSIS MOUNT

J1
J2
W2
W02
W01
0
NC
RPG1
+5.2V
C3 0.01
C25 0.01
C26 0.01
TP2
U8E
U8F

(DEBOUNCE)

U9B (TIMING) TP14 U14D U14C R11 511Ω +6.2VF U4A FF TP15 REPEAT RESET

U8D TP11 C23 0.01

LOW DEBOUNCED KEY DOWN

LOW KEY DOWN

REPEAT DISABLE

Ⓓ REPEAT FUNCTION CIRCUITS

+5.2V R3 162K C7 6.8 U9A (TIMING) TP6 NC C4 0.01 +6.2V

U4B TP7 NC +6.2V R2 000 CR1 R1 6.8M C8 0.022

U5A (TIMING) C3 0.01 C2 0.01 +6.2V U14A

DOWN TIMER

+6.2V R5 28.7 C17 1.0 U20B (TIMING) NC TP13

LOW KEY DISABLE TP12

U19B

LOW REPEAT

Ⓘ SRQ BUFFER

+6.2V U3A U23A 10K TP9 TP10 +I RPG SRQ +I KEY ON SRQ LSRQ J3-45 LSRQ

COUNT WINDOW TIMER

WINDOW

+6.2V R6 48.4K U20A C22 2.2 C21 0.01 (TIMING) NC TP8

Ⓙ INSTR PRESET BUFFER

P1-24 (IN) INSTR PRESET

+6.2V U23E 10K U3D C1 2.2 U23D 10K U3C U23F 10K J3-19 (OUT) LIP5

U2A U8A

Ⓔ ANNUNCIATOR LATCHES

KEYBOARD LOCKOUT

+6.2V U6 C5 0.1 REG DB8 DB9 DB10 DB11 DB12 DB13 DB14 DB15

LSPLD FT-44 U2D U2

U7 C27 0.01 C6 0.1

U16 C15 0.1

INST PR LOCKOUT

U17 C29 0.01 C16 0.1

Figure

1. REFER TO FIGURE 8-8 FOR DETAILED SCHEMATIC DIAGRAM SYMBOLOGY NOTES.
2. RESISTANCE VALUES SHOWN ARE IN OHMS, CAPACITANCE IN MICROFARADS, AND INDUCTANCE IN MICROHENRIES UNLESS OTHERWISE NOTED.
3. THE FRONT PANEL LINE SWITCH IS DOCUMENTED IN DETAIL ON THE A9S RECTIFIER/A10 CAPACITOR SCHEMATIC IN THE POWER SUPPLY SECTION.

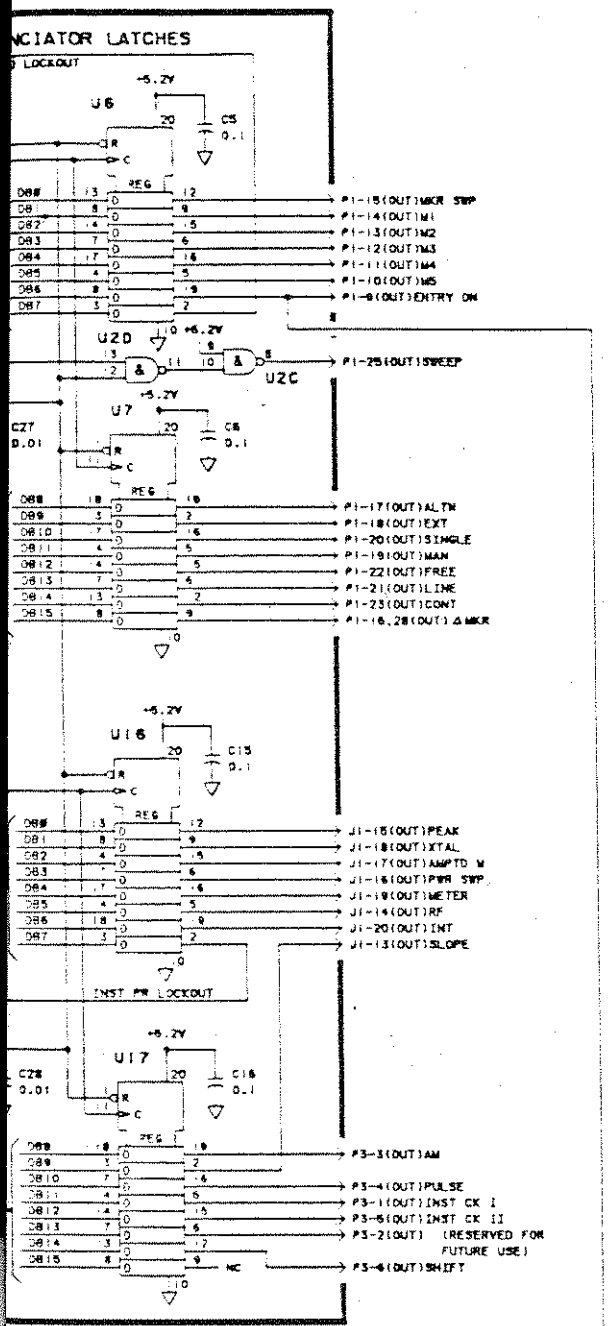
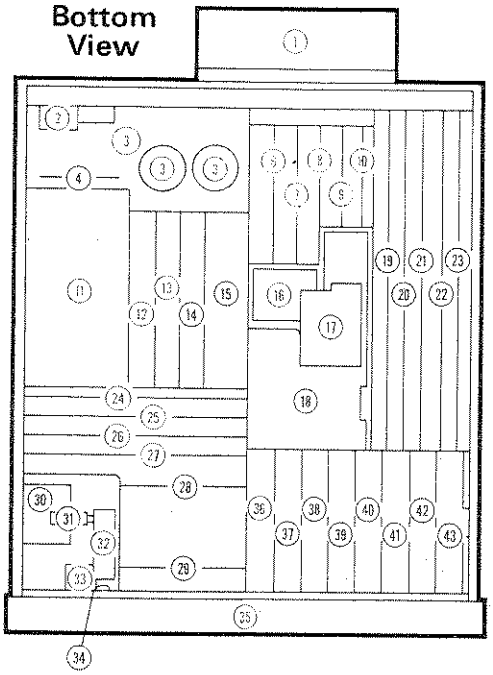
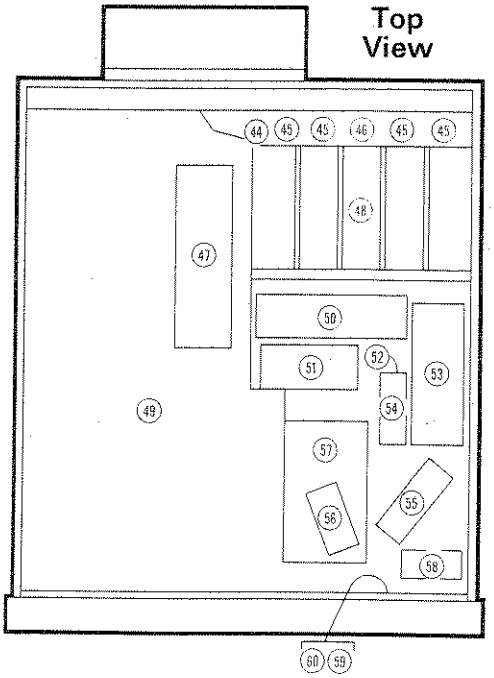


Figure 8-530. A6 Keyboard Interface, Schematic Diagram

NOTES:

REFERENCE GUIDE TO SERVICE DOCUMENTATION





Assy./Ref. Des.	Description	Location	Volume 2: Ref.-M/N Loops	Volume 2: 20/30 Loops	Volume 2: Swp. Gen.-YO Loop	Volume 2: Motherboard	Volume 2: Controller	Volume 3: Front/Rear Panel	Volume 3: RF Section	Volume 3: Power Supplies
A1	Alpha Display	35					●			
A2	Display Driver	35					●			
A3	Display Processor	35					●			
A4	Not Assigned	-								
A5	Keyboard	35					●			
A6	Keyboard Interface	35					●			
A7	Lower Keyboard	35					●			
A8	3.7 GHz Oscillator	57						●		
A9	Band 0 Pulse Modulator	56						●		
A10	Directional Coupler	32						●		
A11	Band 1-4 Detector	31						●		
A12	Band 0 Detector	34						●		
A13	SYTM (Switched YIG Tuned Multiplier)	30						●		
A14	Band 1-4 Power Amplifier	33						●		
A15	Band 0 Low Pass Filter	53						●		
A16	Band 1-4 Modulator/Splitter	51						●		
A17	Band 0 Mixer	54						●		
A18	Band 0 Power Amplifier	55						●		
A18A2	Band 0 Splitter	60						●		
A19	Capacitor Assembly	48							●	
A20	RF Section Filter	50						●		
A21	Pulse Modulator Driver	29						●		
A22	Not Assigned	-								
A23	Not Assigned	-								
A24	Attenuator Driver/SRD Bias	28						●		
A25	ALC Detector	27						●		
A26	Linear Modulator	26						●		
A27	Level Control	25						●		
A28	SYTM Driver	24						●		
A29	Reference Phase Detector	13	●							
A30	100 MHz VCXO (Voltage Controlled Crystal Osc.)	13	●							
A31	M/N Phase Detector	14	●							
A32	M/N VCO (Voltage Controlled Osc.)	15	●							
A33	M/N Output	15	●							
A34	Reference-M/N Motherboard	5	●							
A35	Rectifier	4							●	
A36	PLL1 VCO (Voltage Controlled Osc.)	45		●						
A37	PLL1 Divider	37		●						
A38	PLL1 IF	36		●						
A39	PLL3 Upconverter	36		●						
A40	PLL2 VCO (Voltage Controlled Osc.)	40		●						
A41	PLL2 Phase Detector	41		●						
A42	PLL2 Divider	42		●						
A43	PLL2 Discriminator	43		●						
A44	YIG Oscillator (YO)	12			●					
A45	Pre-Leveler	19			●					
A46	7 GHz Low Pass Filter	18			●					
A47	Sense Resistor Assembly (YO circuit)	47			●					
	(SYTM circuit)	47						●		
A48	YO Loop Sampler	19			●					
A49	YO Loop Phase/Detector	18			●					
A50	YO Loop Interconnect	17			●					
A51	Reference Oscillator	16	●							
A52	Positive Resulator	6							●	
A53	Negative Regulator	7							●	
A54	YO Pretune DAC/Delay Compensation	8			●					
A55	YO Driver	9			●					
A56	-15V Regulator	10							●	
A57	Marker/Bandcross	19				●				
A58	Sweep Generator	20			●					
A59	Digital Interface	21				●				
A60	Processor	22				●				
A61	Memory	23				●				
A62	Main Motherboard	49					●			
A63	70 dB RF Attenuator	52						●		
AT1	Peripheral Mode Isolator	59						●		
B1	Fan Assembly	1							●	
A62C1-3	Power Supply Filter Capacitors	3							●	
FL1	AC Line Module	2							●	
A62Q1-4	Power Supply Regulating Transistors	-							●	
A62S1	Power Supply Thermal Switch	44							●	
T1	Power Supply Transformer	11							●	
A62U1	Power Supply Regulator	46							●	

RF SECTION (POWER LEVEL CONTROL)

ALC LOOP OVERVIEW

The ALC Loop is a feedback control system which monitors RF power and attempts to control that power to a set level. The point at which the power is monitored may be inside the instrument (internal leveling), or the user may choose to monitor power at some point in his test setup, (external leveling). A voltage derived from the power sensor (internal crystal detector, external crystal detector, or external power meter) is compared to a reference voltage at the loop summing point. If the resulting currents at the summing node do not cancel, the loop integrator output voltage will change. This voltage controls the modulator which varies the RF output power. The power will thus change until the voltage representing RF power cancels the reference, at which point, the integrator output stops changing and the power remains constant at its desired level. Fundamentally, the feedback loop is attempting to reduce the current into the integrator to zero. For any given reference voltage there is one detector output voltage which causes zero integrator current, so one may say that the loop is controlling detector output voltage.

The detector output voltage is primarily a function of RF power into the detector, but it also varies with temperature and RF frequency. Thus, forcing the detector output voltage to some particular level does not guarantee that the RF power will remain constant as the temperature, frequency, or lunar phase changes. A 16 dB directional coupler is used to sample the RF output power. It's "coupled arm" produces a signal 16 dB smaller than the level of the outgoing RF power. Any RF power coming into the instrument from the outside is ideally not coupled to the coupled arm at all. The detector is connected to the coupled arm. The 16 dB coupling factor is not perfectly flat (constant as a function of RF frequency), and the coupler does couple some reverse power into the detector. There is a 10 dB step attenuator (max 70 dB) between the coupler and front panel output connector, which is not flat either. Thus, as the leveling loop holds the detector output voltage constant, the RF output power will vary with frequency due to the flatness of the detector, coupler, attenuator, and RF hardware. If plotted on a graph, this variation can be approximated with several straight line segments to within ± 1 dB. Straight line variations can be compensated out by making the reference voltage change as a function of frequency. This is essentially what is done using the "level correction" voltage produced on the A27 Level Control board. The temperature characteristics of the detector are corrected by temperature compensation circuits on the A25 ALC Detector board.

The normal range of power at the output of the coupler is from 0 dBm to -10 dBm. The attenuator is used to get lower powers. For

instance, -56 dBm is achieved with 50 dB attenuation and the ALC loop set to -6 dBm. The loop is not normally set to less than -10 dBm for noise and drift reasons (the detector output is approximately 1 mV for -10 dBm RF output). The maximum attentuation is 70 dB. To get from -80 dBm to -90 dBm, the ALC is run from -10 dBm to -20 dBm, at which point the level accuracy is degraded by ±1 dB. For powers greater than 0 dBm, the ALC Loop is run at the desired power. At some frequencies, the 8340A is capable of producing +20 dBm, the maximum power the ALC can be set to. To get +20 dBm output, the power amplifier is driven into saturation by about 10 dB. Thus, to reduce its output 30 dB (to -10 dBm), the amplifier input must be reduced 40 dB. This is done by the modulators which consists of PIN diodes shunting a transmission line. Another 20 db of range is needed to provide 90% AM capability.

The actual modulator driver has a sensitivity of -0.03 db/mV to reduce noise sensitivity. The 8340A has two RF signal generation paths, one producing .01-2.3 GHz (Band 0), the other producing 2.3-26.5 GHz (Bands 1-4). Each path has its own modulator and crystal detector. For Band 0 the modulator is part of the A8 3.7 GHz Oscillator. For Bands 1 through 4 the modulator is the A16 Band 1 through 4 Modulator splitter. The dual slope logger on the A25 ALC Detector assembly has FET switches at its input to select the appropriate detector. The thermistor used for the detector temperature compensation is physically located inside the LO Band detector housing. This is mounted directly to the high band directional coupler to which the HI Band detector is connected. Thus, the thermistor thermally tracks both detectors. The LO Band detector is designed to have the same temperature drift as the HI Band detector.

The x5 amplifier following the logger has several functions. It has a high input impedance to prevent loading the logging elements. It boosts the signal to a high enough level so that noise, drift, and sample/hold offsets are not a problem. It is capable of driving the Sample and Hold capacitor which follows. It provides a point to add the level correction signal.

The level correction signal compensates for the frequency response of the RF hardware. If the instrument is sweeping frequency, and the modulator is continually adjusted to keep the output power constant, the detector output voltage will not be constant due to unflatness in the attenuator, coupler, detector, and connecting hardware. The level correction signal is made to approximate this unflatness with four straight line segments. This signal gets added to the detector voltage so that the output of the x5 amp is flat with frequency. This voltage is now an accurate representation of the actual front panel output power and is used to drive the front panel level meter as well as close

the feedback loop. The level correction signal could have been added at several other places in the loop but was done here for the benefit of the level meter.

Following the x5 amplifier is a sample/hold circuit which is there primarily for pulse modulation. The 8340A provides internally leveled pulse modulation for pulse widths as narrow as 100 nanoseconds. Since the ALC Loop has a loop bandwidth of 100 KHz (rise time approximately 4 usec), the loop cannot be expected to generate shorter pulse widths. In pulse mode, the linear modulator is held at a fixed level, and another modulator (the pulse modulator) turns the RF ON and OFF with 10 nsec rise and fall times. The ALC circuitry must measure the detector voltage when the pulse is ON and use this information to control the linear modulator. The detector Sample and Hold gate is closed when the RF is ON, open when it is OFF. (The signal controlling the Sample and Hold gate is delayed to account for propagation delays through the logger and amplifier). The Sample and Hold serves to stretch narrow pulses, holding their amplitude during the 10 usec that the integration gate is closed. It also provides a steady voltage to the level meter during pulse operation as well as during RF blanking.

The level meter signal is amplified by a factor of 6.6, to 200 mV/dB. The output of this amplifier is +5.0V at -25 dBm, -5.0V at +25 dBm. This voltage goes to an A to D converter on the A27 Level Control board. The attenuator setting is digitally subtracted from the A to D output and the result displayed on the front panel level meter. When internally leveled, unleveled light not lit, and AM is OFF, this number should agree with the number in the power level entry but may disagree by $\pm$0.1 dB due to component tolerance and drift. Since this is disconcerting to a user, the level meter simply displays the number in the power level entry. The level A to D circuitry is used whenever the actual output power may be expected to differ from the level entry. These conditions are: 1. Unleveled light ON (instrument cannot put out as much power as is requested. The meter displays the actual output.) 2. AM ON (user may put DC into AM input, changing output power.) 3. External leveling selected. (Actual output is a function of the user's detector, coupler, RF hardware, etc.) The x6.6 amplifier contains a 5Hz, active low pass filter, preventing the level meter from flickering for AM rates above 20 Hz.

The output voltage of the logger has a temperature dependence due to its kT/q term. Thus, for constant RF power, the logger output voltage is directly proportional to absolute temperature. (This effect is separate from the detector's temperature drift which is compensated by the thermistor). To maintain the accuracy of the level meter, the gain of the x6.6 amplifier is made to vary

inversely with absolute temperature. This is accomplished by using an input resistor with a temperature coefficient of +3400 ppm/degree C. For the same reason, the ALC reference voltage must be made to increase with temperature at +3400 ppm/degree C so that with constant output power, the logger voltage will track the reference. As long as they track over temperature, the loop will not try to change the power. The reference voltage from the A27 Level Control board is routed through an inverting amplifier on the A25 ALC Detector board whose gain is proportional to absolute temperature. The output of this amplifier goes to the A26 Linear Modulator board where it is fed to the loop summing point. Placing the temperature compensating amplifier on the detector board improves thermal tracking with the logger.

The remaining circuitry on the detector board is for external leveling. The 8340A may use either positive or negative polarity external detectors. The external input goes to an "Absolute Value" circuit which inverts positive inputs but not negative ones. The output of the absolute value circuit drives the external logger. This logger has no special compensation for detector T.C. or square law deviation. Its own inherant temperature drift is compensated by the drifting reference voltage, as for internal leveling. The logger output is amplified by a factor of 10 to 60 mV/dB.

A25 FET switches select either the output of the internal or external circuits to send to the A26 Linear Modulator board. When external crystal leveling is selected, a crossover network consisting of a 1k resistor and .047 uF capacitor is used to help stabilize the loop. Frequencies from DC to about 7 kHz may pass from the external input to the modulator board. Above 7 kHz, the external input is rolled OFF, and the loop is closed through the internal detector via the .047 uF capacitor. In this way, the loop stability is maintained with a wide variety of detector bandwidths. A similar crossover is used for power meter leveling, crossing over at .6Hz.

The external AM input goes to the AM logger on the A26 Linear Modulator board. The output of the logger is amplified by a factor of 10 to 30 mV/dB. This signal is summed into the loop at the same point as the reference causing the loop to change the RF output power accordingly. Since the detector logger has shaped the detector voltage to be linear in terms of decibels, the AM input provides very linear control.

The logged detector voltage, temperature compensated reference voltage, marker signal, and logged AM input are all summed together at the loop summing point. That point feeds the input of an integrator through a FET switch (integrate/hold gate). That switch is normally closed. If it is opened, as between pulses

during pulse modulation, the input to the integrator is zero causing its output to remain constant, thus holding the modulator drive at a constant level. The integrator controls the bandwidth of the leveling loop. The integrator gain is proportional to 1/FC causing gain crossover to occur at F = 130 kHz for C = 1000 pF, and F = 6 kHz for C = .023 uF. The capacitor is selected by a FET switch. The loop is normally in its low bandwidth state, being switched to high bandwidth if sweep times are <5 sec, or AM is ON with pulse mode OFF, or "shift AM" is ON with pulse mode ON.

The integrator output drives an exponential current source Iout = Iin x e10 Iin/1mA. For Iout above 1mA (normal operation), this is a close approximation to an expoential. An exponential modulator drive helps keep loop gain constant as the power level is changed. The input to the current source is controlled by 5 loop gain adjustments selected according to the RF band in use (Band 0, or Bands 1 through 4). The YTM transfer function increases loop gain on its multiplying bands so separate adjustments are necessary. At the output of the current source, an appropriate offset current is subtracted, biasing the current source for a straight line modulator characteristic. The output current is sent to either the Band 0 or Bands 1 through 4 modulator by a pair of FET switches.

When the integrator output is at 0 volts, the modulator will be close to full output. When the loop gain is properly set, the modulator output will decrease at the rate of approximately 30 dB/volt. If increased output power is needed, the integrator moves positive. If more power is needed than the instrument can provide, the integrator will go more positive than the "full on" voltage. At this point, the feedback loop is open, and the integrator will try to saturate in a positive direction. A clamp circuit is activated at approximately +.7V, which dumps current into the integrator input preventing the output from going more positive. Preventing the integrator from saturating greatly speeds recovery time. When the integrator output moves above +.2V, a comparator is tripped which lights the front panel UNLEVELED LED. Another comparator trips for voltages more negative than -3.5V OVERMOD LED, and another clamp is activated at -3.7V.

When RF is turned off during RF blanking, both the pulse modulator and linear modulator are shut down. The linear modulator is used to provide a controlled RF turn-on with no overshoot. This does not happen during pulse modulation because the RF is not off long enough (10 msec. max) for the Sample and Hold circuits to drift. Also, during external leveling, a slow detector would cause turn-on overshoot if the RF were not brought up slowly. The RF on/off control (HRFON) is fed to the clamp circuits in such a way as to force the integrator output to

-3.0V. Note that this will not trip either comparator. When RF is turned on, the voltage rises at the slew rate of the integrator. If external power meter leveling is selected, a capacitor is switched into the RF on/off circuit slowing the turn-on to two seconds.

For troubleshooting purposes, the ALC Loop may be broken and a signal injected to be traced around the loop. When the test mode is activated, the FET switches will be switched to break the connection from the A25 ALC Detector board to the A26 Linear Modulator board. A resistor is switched across the integrator capacitor on the A26 Linear Modulator assembly converting this stage to an inverting amplifier. Thus, the integrator output may be smoothly controlled via the reference DAC. The signal may then be traced from there to the modulator driver, RF output, detector output, logger output, x5 amp, through the Sample and Hold, level amp, and to the A to D driving the level meter. By putting a detector on the RF output, the external leveling circuits may be excersized.

To enter the test mode, press INST PRESET, cw, and SHIFT METER. The UNLEVELED LED should be ON. The POWER dBm display should indicate the approximate RF output power. The ENTRY DISPLAY should indicate ''ATN: -00, MOD: 0.0 dB''. The modulators are being controlled by the voltage at A26TP3. This voltage is programmed by the ALC Reference Generator DAC on the A27 Level Control assembly. The DAC can be controlled using the RPG. Rotate the RPG ccw and note that the ENTRY DISPLAY MOD level changes. Continue turning the RPG ccw until the Power dBm display begins to change. The absolute MOD level indication is not important, however, a further decrease in MOD level should generate a corresponding decrease in the Power dBm display and the RF output power (i.e., 10 dB MOD level change should generate 10 dB $\pm$3dB power change). A defective circuit can be isolated by turning the voltage from A26TP3 to the modulators or by tracing the RF path from the YO to the Level Meter Amplifier on the A25 ALC Detector assembly. The AM signal path must be checked separately.

SYTM PEAKING

SYTM Peaking is a function designed to tune the SYTM such that the RF signal (YO frequency or multiple of the YO frequency) is in the center of the SYTM 1dB pass band insuring that maximum RF power is available.

The peaking routine is stored in ROM and can be accessed manually by pressing the front panel PEAK button or remotely by a "RP1" instruction. An "RP0" instruction will remotely turn OFF the peaking function. The peaking routine when accessed in this manner will execute only if the 8340A is in CW or MANUAL mode and if the RF is ON.

By manually pressing SHIFT AMPT MKR or remotely programming "SH AK", the peaking function will execute immediately even if not in the CW or MANUAL mode; however, only a fine search around the most recent slope DAC (A28U24) setting will be done. Since the SYTM passband is not tuned to track the output frequency in Band 0 (heterodyne band) the peaking routine will not execute if Band 0 is selected.

The ALC detector monitors the RF output level. The detected level is routed to the A25 ALC Detector Board. The DET OUT output (A25P1 Pin 32) is fed to the A26 ALC Modulator (A26P1 Pin 10). The MOD LVL (A26P1 Pin 32) is then fed to the A27 Level Control Board (A27P1 Pin 61) where it becomes one input to the ADC Input Multiplexer. The peak routine programs the ADC Multiplexer to route the MOD LVL voltage to the Test ADC. By monitoring the Test ADC output while tuning the SYTM the program can find the peak RF signal level.

The SYTM is tuned by varying the slope DAC setting. When the peak function is activated on the front panel, the 8340A will do a full peak (i.e.,coarse and fine search) if in CW or MANUAL. If the peak function is left ON, the 8340A will repeak every 7 minutes doing only a fine search around the most recent slope DAC setting. If the CW or MANUAL frequency is changed while peaking is ON using the RPG a fine search around the most recent slope DAC setting will be done; however, if the CW or MANUAL frequency is changed using the step keys or numerical entry keys, a full peak will be done.

The MOD LVL voltage is offset and scaled so that the 10 volt input range of the ADC covers MOD LVL voltages between -3.53 V to +2.47 V. The input range is equivalent to about 6 mV/bit. The sensitivity of the MOD LVL line is around 20 to 50 mV/dB so the ADC has a sensitivity of about 0.2 dB/bit.

The SYTM passband has a second narrower peak that is located

200-300 MHz lower in frequency than the desired peak. The coarse search routine starts at the top of the passband and searches for a peak in 15 MHz steps. Once a peak is found the coarse search continues for another 150 MHz to verify that the correct peak is found and stops before the second peak is reached. 15 MHz was chosen for the step size because the minimum 1dB bandwidth is 24 MHz so at least one of the steps will fall within 1dB of the peak. Once the coarse search peak is located, the processor takes a reading of the modulator level to be used as a reference for the -1dB points. The level control DAC (A27U14) is then stepped down 1dB which causes the modulator level to drop 1 dB (since the ALC loop must generate the 1 dB change). The processor then uses the -1dB reference and steps the slope DAC up until the modulator level is equal to or less than the -1dB reference level. The slope DAC is then stepped down from the peak until the same reference threshold is reached. If the slope DAC goes out of range before the -1dB reference level is reached, the routine searches the other side of the passband to the same modulator threshold present when the slope DAC reached the end of its range. The slope DAC is then set to the midpoint of the two values it had when the reference level was reached and the original power is restored. The setting for the slope DAC can be accessed by doing an IO read from subchannel 10.

Peaking is done at the current ALC power level because the SYTM passband may vary with power level. In the fundamental band, the YIG sphere in the SYTM may squeg if too much power is applied. To prevent this from interfering with peaking, the maximum ALC power setting (in the fundamental band only) is 0 dBm during the coarse search and +10 dBm for the fine search. Once the peaking is completed, the original power is restored.

When the instrument goes unleveled, the current driving the ALC modulator is turned off to give maximum available power. However, the MODLVL line has a soft clamp that still gives an indication of the dtected power out of the SYTM with a sensitivity of 20 to 50 mV/dB. The absolute power level shifts by about 1 volt when the instrument goes unleveled but the incremental level remains valid. The absolute level shift poses no problem to the peaking routine since the peaking routine uses incremental changes.

If the FAULT LED comes on the function that caused a fault can be determined by pressing the SHIFT key and then the MANUAL SWEEP key. If the peak indicator is flaching, it means that the peaking routine failed to find a peak within the range of the SYTM slope DAC. This can be caused by several different problems: the SYTM driver may not be shifting the passband, there may not be enough power out of the SYTM for proper ALC operation, the ALC modulator might be defective or the ADC might be defective. Looking at the CMP test point on the A28 SYTM Driver board will give an

indication of how the slope DAC is varying. This trace can be compared with the A-to-D IN test point on the A27 Level Control board to see if the A-to-D input is reasonable. If the voltage on the A-to-D input doesn't trace out a passband as the slope DAC is varied, check the MODLVL test point on the A26 Linear Modulator board. The A-to-D IN test point should be a scaled bersion of the voltage at the MODLVL test point. If the fault is due to peaking, the fault light may be cleared by pressing the INSTR PRESET key or by turning the line power off and on.

SYTM tracking is accomplished by pressing SHIFT PEAK on the front panel or by remotely programming ''SH RP'' over the HP-IB bus. SYTM tracking updates calibration constants 9 through 12 to the best value for the SYTM tracking in each band. Each band is tracked independently of the other bands. To track a band, a single band sweep is set up and the sweep is stopped at several points across the band that each sweep is peaked. The number stored in the calibration constant represents the least squares fit to the slope DAC numbers returned from the peaking routine with the lowest power point receiving a double weighting. If the least squares number is out of the range of the slope DAC, the fault light is turned on with the TRK indicator flashing when SHIFT MANUAL is pressed. In Band 1, the SYTM is peaked at 2.3 GHz and at one GHz steps from 3 GHz to 7 GHz. In Band 2 the SYTM is peaked at 6.9 GHz and at one GHz steps from 7.5 to 13.5 GHz. In Band 3, the SYTM is peaked at 13.4 GHz and at one GHz steps from 14 GHz to 20 GHz. In Band 4, the SYTM is peaked at 19.8 GHz and at one GHz steps from 20.5 GHz to 26.5 GHz.

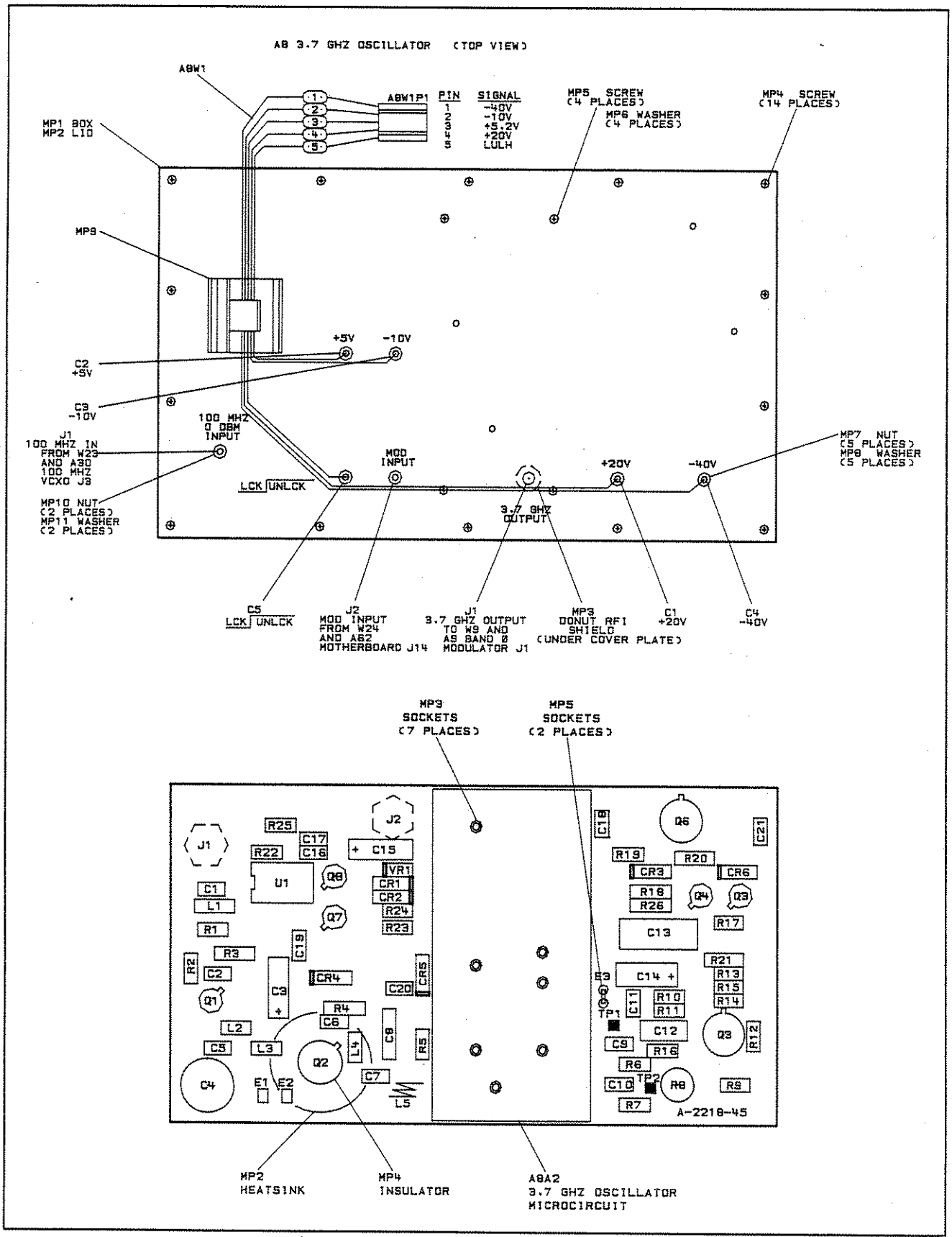


Figure 8-566. A8 3.7 GHz Oscillator, Component Location Diagram

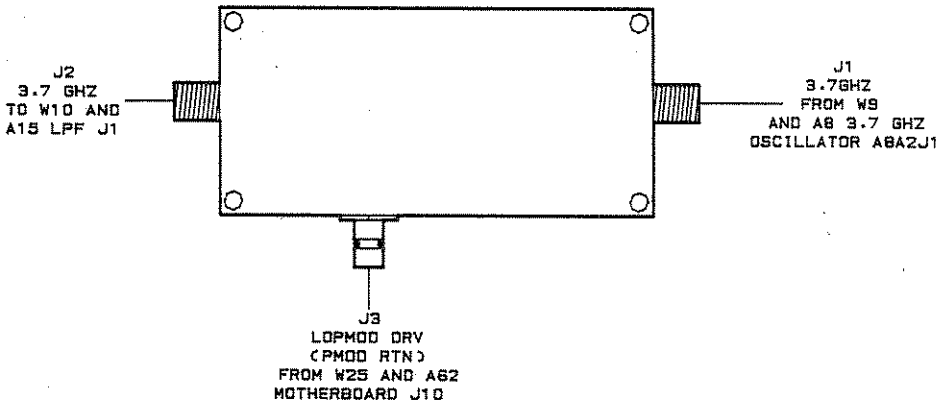


Figure 8-573. A9 Band 0 Pulse Modulator,
Component Location Diagram

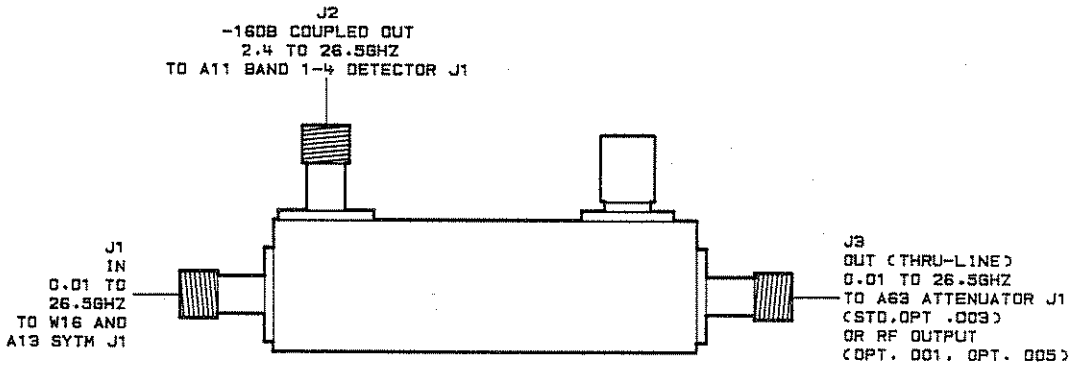


Figure 8-578. A10 Directional Coupler,
Component Location Diagram

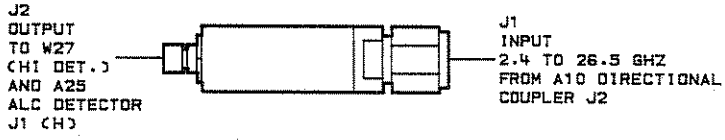


Figure 8-583. All Band 1-4 Detector,
Component Location Diagram
8-329/8-330

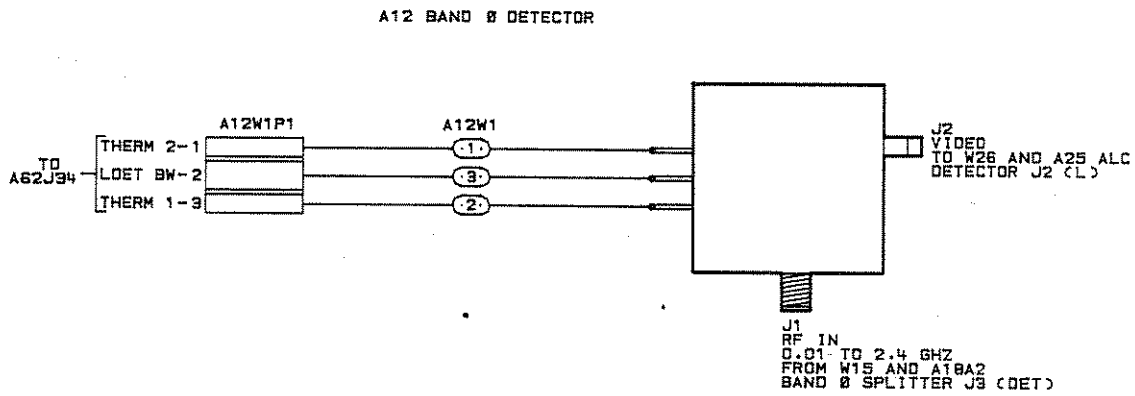


Figure 8-588. A12 Band 0 Detector,
Component Location Diagram

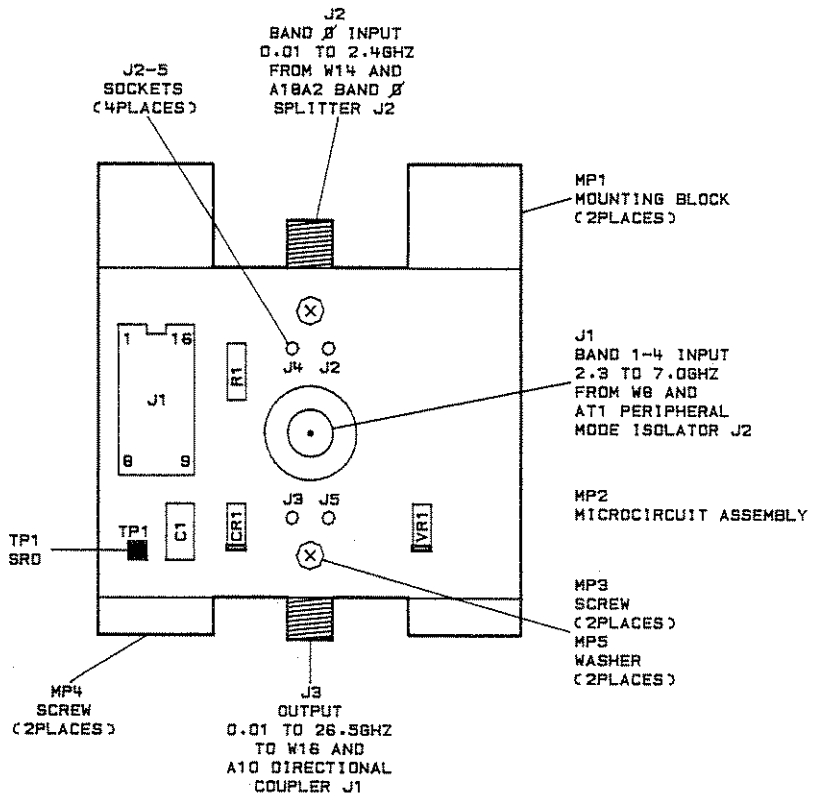


Figure 8-594. A13 SYTM, Component Location Diagram

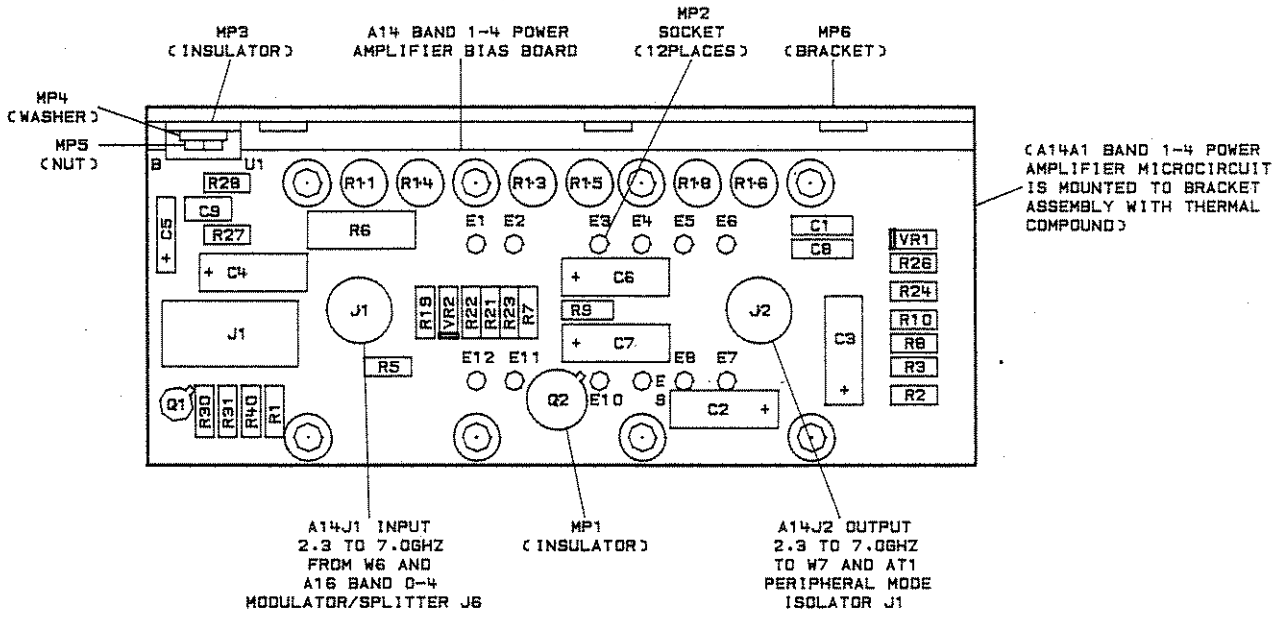


Figure 8-600. A14 Band 1-4 Power Amplifier,
Component Location Diagram
8-335/8-336

Figure 8-607. A15 Band 0 Low Pass Filter,
8-337/8-338

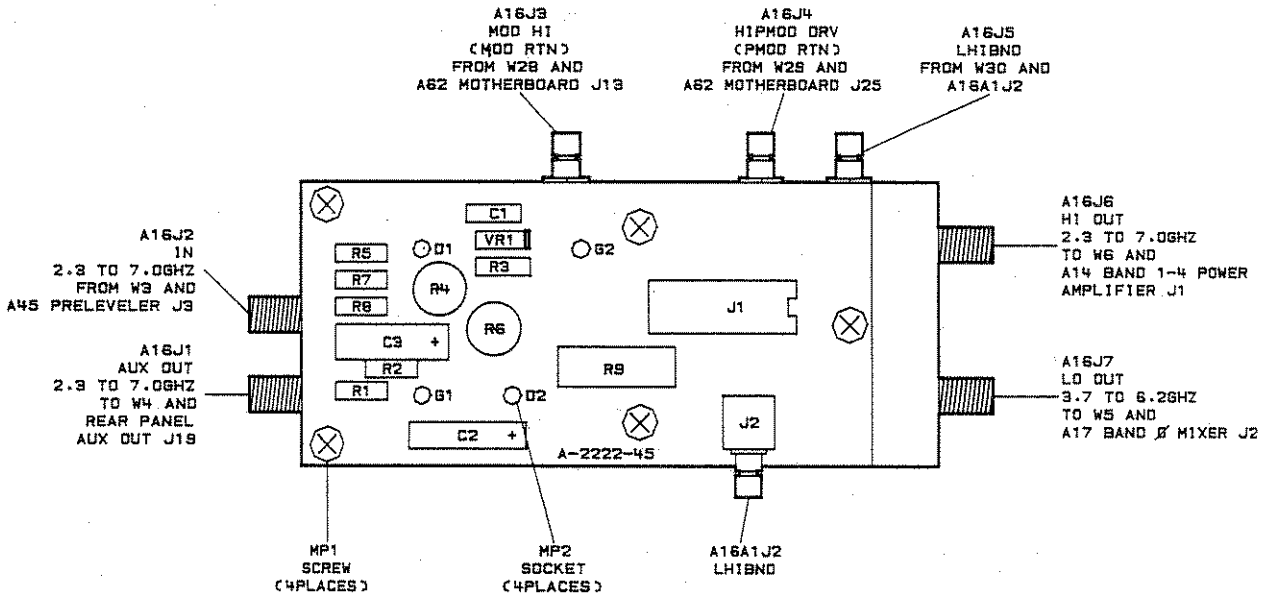


Figure 8-612. A16 Band 1-4 Modulator/Splitter, Component Location Diagram

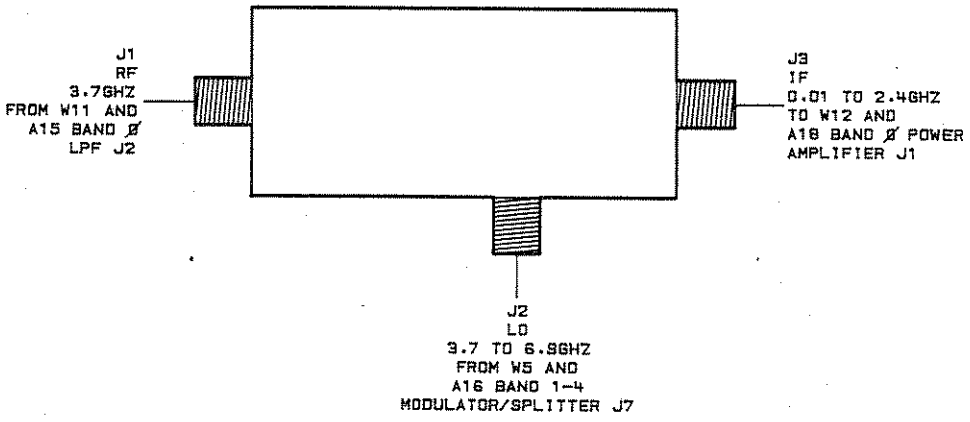


Figure 8-619. A17 Band 0 Mixer,
Component Location Diagram
8-341/8-342

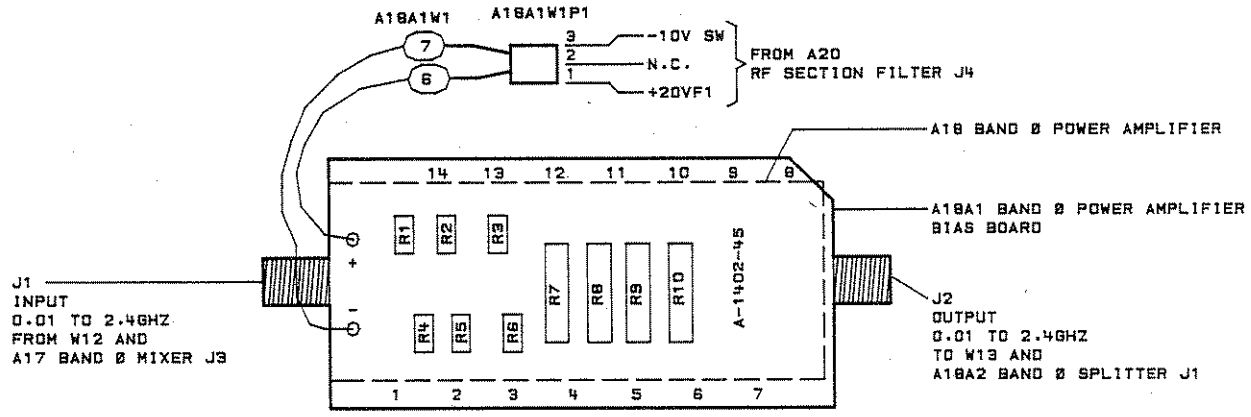


Figure 8-624. A18 Band 0 Power Amplifier, Component Location Diagram

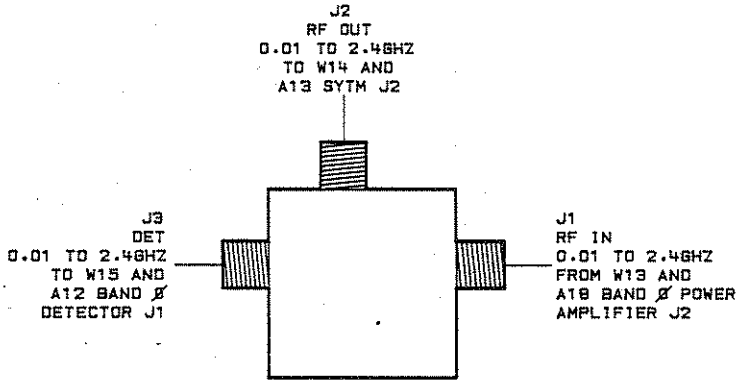


Figure 8-626. A18A2 Band 0 Splitter,
Component Location Diagram
8-345/8-346

A20 RF SECTION FILTER, CIRCUIT DESCRIPTION

Introduction

The RF Section Filter consists of the following major sections:

* Power Amplifier Supply Filters
* Low Band Amplifier Switch.

Power Amplifier Supply Filters

The A14 Band 1-4 Power Amplifier draws a fairly substantial amount of current from the +5V and -10V supplies when it is operated at full power. During Pulse operation the input to the Power Amplifier is turned on and off at the pulse rate. This large surge current, if it is allowed to get back to the power supply, would cause the power supplies voltage to fluxuate at the pulse rate. This is true because the pulse rate is normally at a higher frequency than the Power supplies bandwidth. These voltage fluxuations would get into the Phase Lock Circuitry or main YO Coil Driver circuitry and cause large side bands on the output carrier at the frequency of the pulses.

In order to minimize this effect, a two stage LC filter is used in both the +5.2V and -10 V supplies going to the A14 assembly. The capacitors are large (100 uF) and the inductors are just 18-20 turns of wire wound on a lossy toroid core.

Low Band Amplifier Switch

The Band 0 Power Amplifier is turned off when the low band is not selected. The amplifier is turned OFF by removing the -10V to the amplifier. The circuit that does this resides on the RF Filter Board. When the signal LHET is LOW indicating that the instrument is operating in the low band (Band 0), Q1 is biased ON via the voltage divider formed by R2 and R3. The collector of Q1 is pulled up to ground and Q2 is biased on Via the voltage divider formed by R4 and R5. Q2 is saturated and pulls its collector down to -10 V and thus turns on the Low Band Amplifier. When LHET is HIGH Q1 is biased off which biases Q2 off and therefore its collector is left floating which turns off the Low Band Amplifier. The -10 V input to this switch is derived from the filtered -10 V supply that is also used by the High Band Amplifier.

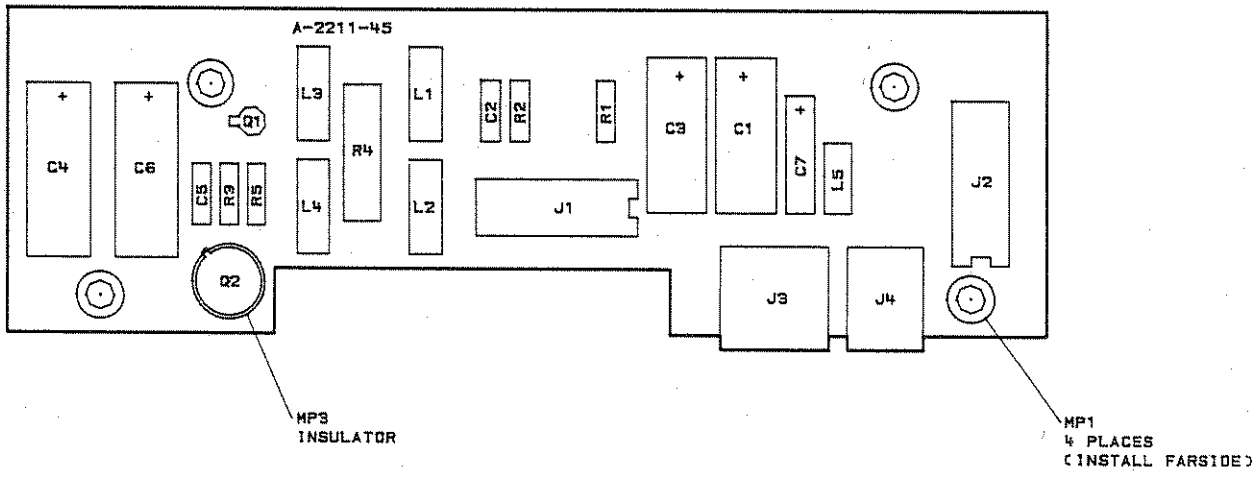


Figure 8-631. A20 RF Section Filter,
Component Location Diagram

Figure 8-633. RF Section, Schematic Diagram

The RF Section Schematic Diagram is contained in an envelope inside the rear cover of Volume 3.

A21 PULSE MODULATOR CIRCUIT DESCRIPTION

Introduction

The A21 Pulse Modulator assembly controls the pulse modulation functions for the 8340A. The front panel BNC "PULSE MODULATION INPUT" is the main control signal. The A21 Pulse Modulator then drives the PIN switch RF modulators in the A9 (for Band 0) or A16 (for Band 1-4) microcircuits. In addition, timing circuits send controls signals to key elements of the ALC loop to coordinate the leveling function with the pulse modulation.

Input Buffer and Control Logic A

The input buffer (Q7 circuit) buffers the "PULSE MODUATION INPUT" (TTL compatible (high = RF on; low = RF off), and protects Q7 from higher input voltages. Two control lines gate the pulse input. HPLSEN gates the buffered pulses (high = Enabled; low = Disabled). HRFON overrides the pulse input, causing the RF to be turned off (high = RF on; low = RF off). TP5 is the assembly's primary gated control line (high = RF off; low = RF on).

With no input signal CR1 is forward biased, Q7 is on and U1C pin 10 is low. During the low state of an input signal, CR1 is turned off, Q7 is off and U1C pin 10 is high. The output of U1C (pin 8) will not go low unless HPLSEN is high. If either input to U1B is low the RF is turned off.

The input impedance is established by R14. If necessary R14 can be changed to 51.1 ohms to provide a 50 ohm input impedance. However, if R14 is 51.1 ohms, with no input signal CR1 is not forward biased, Q7 will be off and U1C pin 10 will be high. Now if HPLSEN is high (front-panel PULSE key on) the RF will be turned off.

Modulator Driver B

The Modulator Driver provides the current and voltage bias for the RF pulse modulators, controlled by TP5. Differential current switch Q2 and Q3 control the bias for the drivers Q5 and Q8. With TP5 high (high = RF off), Q2 is off and Q3 is on, sourcing current through CR4 and CR5. This turns Q5 on, sourcing 20mA through R11 to bias the PIN diode modulator on, turning the RF off. With TP5 low (low = RF on), Q2 is on and Q3 is off. Now the drivers are biased through CR8, CR3, CR4, CR6, and R10 to -10VF. This turns Q8 on, back-biasing the PIN diodes off and turning the RF on. C3 and C4 AC-couple the transition current spikes from the modulators back to the A21 assembly.

Output Multiplexer C

The Output Multiplexer selects one RF modulator to receive the pulse modulation control. With LHET low (low = Band 0), U3D and U3C turn Q12 on and Q11 off, selecting A9 (Band 0) to pulse modulate. With LHET high (high = Band 1-4), Q12 is off and Q11 is on, pulse modulating A16 (Band 1-4). U3B biases A16 off when HRFON is low (low = RF off) when the front panel "RF" is off and during retrace.

ADC Timing D

The ADC Timing enables the ADC (A27) to monitor the detected power level when either the RF is on or up to 1 millisecond after the RF has been turned off. This is to prevent the "POWER dBm" display from showing an invalid power level if the RF has been turned off for over 1 millisecond (ALC Sample/Hold droop). With TP5 low (RF on), TP3 is forced high to enable the ADC. When TP5 goes high, one-shot U2B is triggered to output a 1 millisecond low pulse, holding the ADC enabled. If the RF is not turned on again within 1 millisecond, U2B returns high, forcing TP3 low to disable the ADC.

Integrator Timing E

The Integrator Timing controls timing to gate the integrator input of the main ALC amp (A26), ensuring that the integrator responds to RF power level error signals only when the RF level detected is on and stable. When TP5 goes low (RF on), U1A output is forced high. The following low-pass filter section delays the transition by 1 microsecond. When TP2 goes high, the integrator (A26) is enabled. When TP5 goes high again (RF off), U1A output goes low to put the integrator circuits into hold. One-shot U2A is triggered when TP5 goes low, outputting a low pulse to U1A. This determines the minimum time that TP2 is high (integrate) for each RF pulse with very narrow pulse widths. The one-shot time period depends on the ALC loop bandwidth and is controlled by HLBW. With HLBW high, the minimum sample time is 1 microsecond; with HLBW low, the minimum sample time is 10 microseconds.

Sample/Hold Timing F

The Sample and Hold Timing controls timing of sample/hold gate in detector circuits (A25) during pulse modulation. The key timing element is C13. The time delay constant is independent and adjustable for both RF on and RF off. The voltage on C13 is detected by Schmitt trigger Q6/Q9. The squarewave output is then delayed from the pulse at TP5, with both leading and trailing edges delayed by independent and adjustable time periods.

The circuit functions as follows: Presume C13 to be charged. When TP5 goes low (RF on), Q1 turns off, and C13 discharges through R24, R23, R22, and R21. R21 adjusts the "ON DELAY" (discharge).

When the voltage on C13 reaches the lower threshhold, Q6/Q9 fires and TP1 goes high to sample. When TP5 goes back high (RF off), Q1 turns on, and charges C13 through R23 and R24. R23 is adjustable and controls the "OFF DELAY" (charge). When the voltage on C13 reaches the upper threshhold, Q6/Q9 fire and TP1 goes low to hold. If C13 is not fully discharged before TP5 goes high again, the rising edge of TP5 will turn on Q4 very briefly through C12 to fully discharge C13. This ensures that the "OFF DELAY" is independent of pulse width.

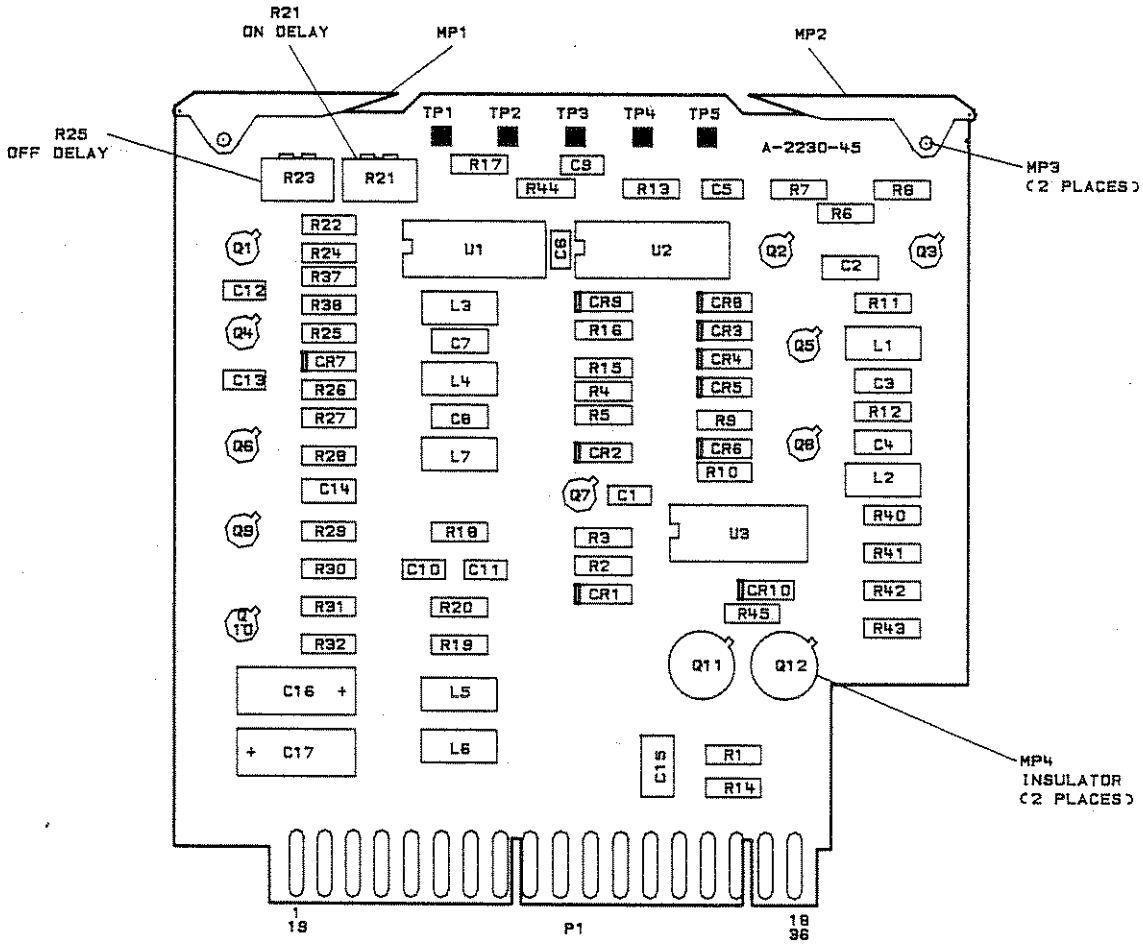


Figure 8-637. A21 Pulse Modulator Driver,
Component Location Diagram

A21 PULSE MODULATOR DRIVER
08340-60024

PULSE MODULATION INPUT

FRONT PANEL J2 — J2P1 — PLS IN

P/O A62 MOTHERBOARD J26 — XA21

P1 — 18 PLS IN — 17 PLS IN RTN

TTL

(A) INPUT BUFFER AND CONTROL LOGIC

+6.2V — C15 0.1

R1 3160 — CR1 — R2 511

R14 100K NOTE 3

+5.2VF — R4 1000 — Q7 — R3 1000

R5 1000 — CR2

C1 18pF

U1C — U1B

-5.2VF — R37 619 — R38 1780

TP5 +3.7 +0.4

L PLSON

P1-9(IN)HPLSEN

P1-27(IN)HRFON

(B) MODULATOR DRIVER

+6.2VF — R6 196

Q2 — Q3

C2 0.1

+2.4 -1.4

CR3 — CR8 — CR5

R9 196

(D) ADC TIMING

+6.2VF — R13 100K — C5 .022 — U2B

EXTERNAL TIMING

L PLSON — +5.2VPU

(E) INTEGRATOR TIMING

+5.2VF — R17 51.1K — C8 470PF — U2A

+5.2VF — R15 1330 — CR9

P1-6(IN) HLBW — R16 3480

EXTERNAL TIMING

L PLSON — +5.2VPU

(G) POWER SUPPLIES

P1-4,22(IN)+20V — +20V

P1-5,23(IN)+6.2V — L5 15 — C16 33 — R44 1000 — +6.2VF — +5.2VPU

P1-7,25(IN)-10V — L6 220 — C17 6.8 — -10VF

P1-8,26 GND

DATE CODE: A-2230-45 17 SEPT 82

1. REFER TO FIGURE 8-X FOR DETAILE SCHEMATIC DIAGRAM SYMBOLOGY NOTES.
2. RESISTANCE VALUES SHOWN ARE IN C CAPACITANCE IN MICROFARADS, AND INDUCTANCE IN MICROHENRIES UNLES OTHERWISE NOTED.
3. R14 CAN BE REPLACED BY A 51.1 OH RESISTOR TO TERMINATE THE PULSE MODULATION INPUT IN 50 OHMS. REFER TO TEXT.
4. Q11 AND Q12 TOP VIEW:

5. CONDITIONS FOR WAVEFORMS TO BE SPECIFIED IN FINAL MANUAL.

Figure 8-639. A21 Pulse Modulator Schematic Diagram

NOTES:

NOTES:

1. REFER TO FIGURE 8-X FOR DETAILED SCHEMATIC DIAGRAM SYMBOLOGY NOTES.
2. RESISTANCE VALUES SHOWN ARE IN OHMS, CAPACITANCE IN MICROFARADS, AND INDUCTANCE IN MICROHENRIES UNLESS OTHERWISE NOTED.
3. R14 CAN BE REPLACED BY A 51.1 OHM RESISTOR TO TERMINATE THE PULSE MODULATION INPUT IN 50 OHMS. REFER TO TEXT.
4. Q11 AND Q12 TOP VIEW:

5. CONDITIONS FOR WAVEFORMS TO BE SPECIFIED IN FINAL MANUAL.

Figure 8-639. A21 Pulse Modulator Driver, Schematic Diagram

A24 ATTENUATOR DRIVER/SRD BIAS, CIRCUIT DESCRIPTION

Introduction

The A24 assembly has two primary functions. One is to control the 70 dB RF step attenuator. The other is to supply the correct bias voltage to the Step Recovery Diode (SRD) in the A13 Switched YIG-Tuned Multiplier (SYTM). The optimum bias voltage is a function of both RF power level and frequency, and also depends upon the frequency band being used. In addition, a simple circuit provides the correct bias for the PIN Diode switch in the A13 SYTM to select Band 0 or Band 1-4.

Frequency Ramp Generator A

The Frequency Ramp Generator provides two frequency-tracking ramp voltages for the frequency-dependent element of the SRD bias circuits. A 1.4V/GHZ signal is generated on the A28 assembly and follows frequency (P1 pin 6). U1A amplifies and offsets this ramp to produce a decending ramp at TP4. This ramp is again offset and inverted to produce an ascending ramp at TP5. These two opposing ramps are each attenuated through variable resistors and then summed together to form a new ramp in Block B.

Modulator Voltage Clamp B

This circuit generates a voltage dependent on RF power level. Optimum SRD bias depends heavily upon RF power level to the A13 SYTM. SRD BIAS CONT from A26 supplies this information for the SRD bias adjustments. However, when the ALC loop goes unleveled, the SRD BIAS CONT line moves abruptly positive and no longer represents RF power level. The Modulator Voltage Clamp adds two frequency-dependent voltage ramps to this signal. The offsets are adjusted such that when the SRD BIAS control jumps positive, the base-emitter junctions of Q1, Q2, and Q3 become reverse-biased, breaking the connection between SRD BIAS control and the SRD BIAS.

Band Decoder C

The Band Decoder provides control signals based upon the frequency band being used. HLB0, HLB1, and HLB2 are encoded with the current band. They are decoded by U5 into five distinct control lines (TP6 through TP10). Three of these control open-collector comparators to drive FETs which control SRD bias. Two of the comparator outputs are in the SRD Bias Amplifier to select reverse-bias in Band 0, forward-bias in Band 1, and the freqency- and power-dependent bias in Bands 2, 3, and 4.

SRD Bias Adjustments D

The SRD Bias Adjustments circuitry provides the frequency and power-dependent bias adjustments for the SRD in Bands 2-4. Three identical circuits, each with three adjustments, sum together a synthesized control signal. Only one of these three circuits is used at a time, dependent upon the band being used, as switched by the FETs. In each section, two adjustments add currents proportional with frequency to Block D's output current; a third adjustment subtracts current proportional to the RF power level through a transistor controlled by the Modulator Voltage Clamp circuit (Block B).

Exponential Generator E

The Exponential Generator shapes the current generator by the SRD Bias Adjustments circuitry to produce an exponentially shaped current output. Dual transistor Q7 is responsible for the exponential relationship of collector current being an exponential function of base-emitter voltage. The use of a positive coefficient resistor as well as a dual transistor helps cancel out thermal effects. The resulting output is a current sink which is an exponential function of the current input.

SRD Bias Amplifier F

The SRD Bias Amplifier converts the exponential current to a voltage that is fed to the SRD; it also establishes bias for special cases of Band 0 and Band 1. U3 converts the current sunk by the Exponential Converter to a voltage. The MIN adjustment determines the minimum bias voltage (about -0.5V) for very low power levels when the input current is zero. In the special case of Band 0, the L0 line is pulled low, sinking current through R34 and forcing the voltage at TP12 to about +7V. This reverse biases the SRD, attenuating the Band 1-4 RF path. In Band 1, the L1 line is pulled low, turning off Q8 and pulling about 5 milliamps through R35. This forward biases the SRD and allows the fundamental frequency to pass through the SYTM easily while minimizing harmonics. In Bands 2-4, Q8 is turned on and the exponential bias shaping previously discussed is used to bias the SRD.

PIN Diode Bias G

When Band 0 is selected, the PIN diade in the SYTM is reverse-biased, thus allowing the Band 0 signal to pass through the coupling loop to the output of the SYTM. When Band 1-4 is selected, the PIN diade in the SYTM is turned on, grounding one side of the output coupling loop. This is necessary for efficient coupling from the YIG sphere and helps attenuate any stray signals in the Band 0 path. Comparator U12B controls the bias

applied to the cathode of the PIN diode in the A13 SYTM. The PIN diode is biased off (TP11 +12V high) when Band 0 is selected and biased on (TP11 -10V low) when Band 1-4 is selected.

Read Status Output Buffer H

Several status lines are provided in the RF section which may be used to communicate information back to the instrument processor. Most of these lines are not used at present but may be used to provide information to the processor about the operating condition of PC boards in the RF section. This output buffer (U14) is a six bit tri-state buffer which is enabled by the RSTATUS strobe (15,R3:) from the Address Decoder on the A24 assembly. The enable line has a pullup to prevent this buffer from being enabled when the A27 Level Control board is removed.

Attenuator Control Latch I

The Attenuator Control Latch (U13) is a 74LS175 latch which has both inverting and non-inverting outputs for each of four latched inputs. Data bits 10 through 13 are latched from the instrument data bus when the WLEVEL strobe (10:R1:) goes low, then high. A pull-up is provided on the WLEVEL strobe to prevent inadvertent writes if the A27 Level Control board (source of the strobe) is removed. Each data bit latched is used to control one of four attenuator sections. The non-inverting output of each bit is used to activate the driver which removes the attenuator card and inserts the through card for that section. The inverting output is used to activate the driver which removes the through card and inserts the attenuator card. The required inputs (DB 10 through DB 13) to select each attenuation (0 to 70 dB) is shown in a table on the A24 schematic.

Attenuator Coil Drivers J

The A63 Attenuator contains four attenuator cards (10 dB, 20 dB, 30 dB, 30 dB) and four through cards. Each section can switch in an attenuator card or a through card depending upon the total attenuation desired. These sections are switched in by latching solenoids. Once the actuator reaches full travel, the solenoid coil is de-energized by opening contacts internal to the attenuator. Each coil draws 300 milliamps for approximately 8 milliseconds until the internal contacts open the coil circuit. Since each attenuator card requires two solenoids, there are a total of eight separate coils that must be driven at various times, depending upon the section switched and whether a through card or attenuator card is being inserted.

The coil drivers (U8, U9, U10, and U11) are 75451B peripheral positive-AND drivers. These devices are capable of driving 300 milliamps with a saturation voltage of less than 0.7 volts which

is sufficient to drive the 5 volt coils of the attenuator. These drivers do not have diode protection to prevent damage from inductive kick back by the coils. For this reason a TID 125 array of diodes (U13) is connected to provide diode clamping to both ground and to +5.2 volts.

Since the peak current that must be provided to the attenuator and drivers is quite large, a separately filtered power source is provided for this circuitry via L5, C10 and C11 (Block L). The above filtering will prevent current transients from disturbing other functions on this P.C. board.

SYTM Heater Control K

In order to provide a reasonably constant temperature for the micro-circuit inside the A13 SYTM, a heater (resistor) and a thermistor are installed inside the A13 SYTM.

The A13 SYTM heater circuit uses the thermistor inside the A13 SYTM to provide a voltage that changes as the temperature inside changes. This voltage is compared to a reference voltage and amplified by an op-amp (U4). The inverting input of this op-amp is referenced to -5 volts to set the operating point of the amplifier. The -5 volts is obtained from the divider formed by R50 and R51.

As the temperature inside the A13 SYTM rises, the thermistor resistance decreases, thereby increasing the voltage at TP2 since the thermistor forms the upper leg of a resistive divider between ground and -10 volts. R48 is the input resistor to the op-amp and when the above voltage increases, the voltage at the op-amp output (U1 pin 6) increases, which decreases the current to the base of Q1. This decreases the amount of current provided to the A13 SYTM heater and thus decreases the temperature. Feedback is provided around this circuit by R49 and C13. This feedback allows a very large gain at DC and sets a gain of 30 at frequencies above a few hundredths of a Hertz.

If the temperature inside the A13 SYTM decreases, the opposite occurs and the heater circuit increases the current to the heater. This circuit is designed to maintain the temperature of the YIG sphere at approximately 85 degrees Centigrade independent of the ambient temperature.

Power Supply L

An LC filter circuit is used on each power supply line. The component values for these filters were chosen to form a low Q circuit to reduce any chance of resonances.

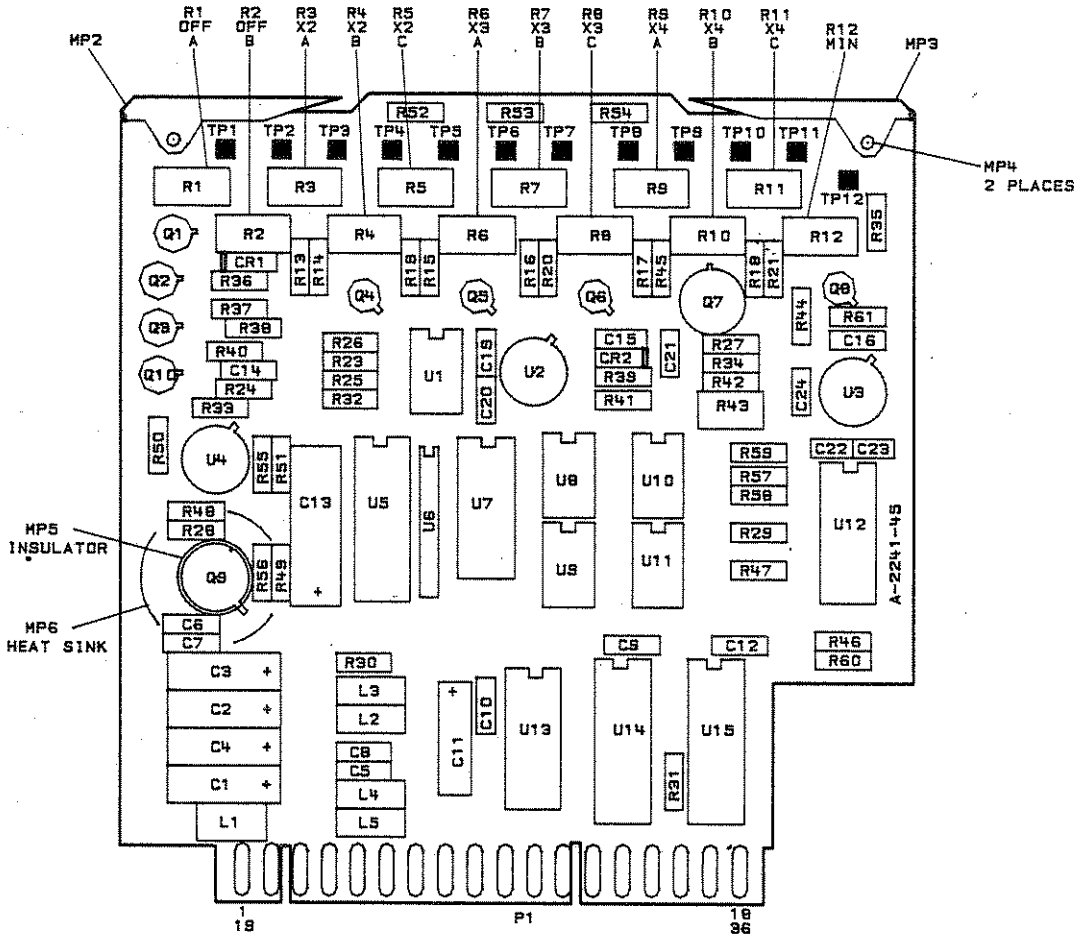
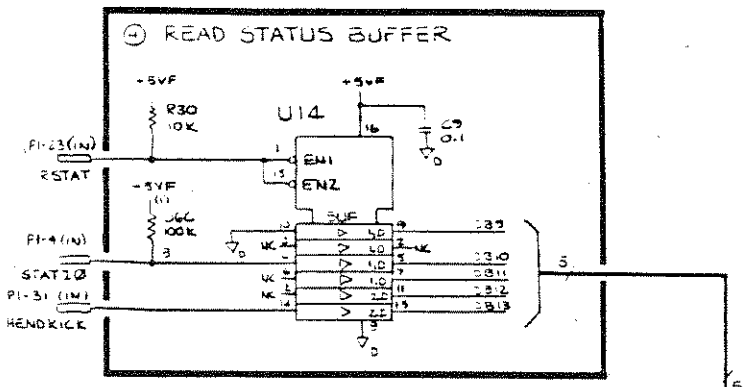
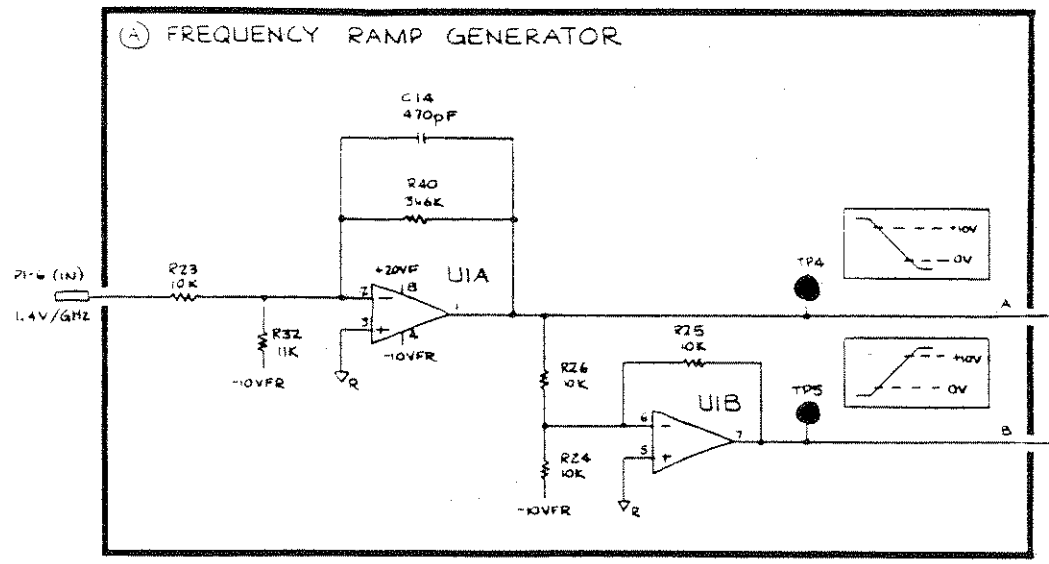
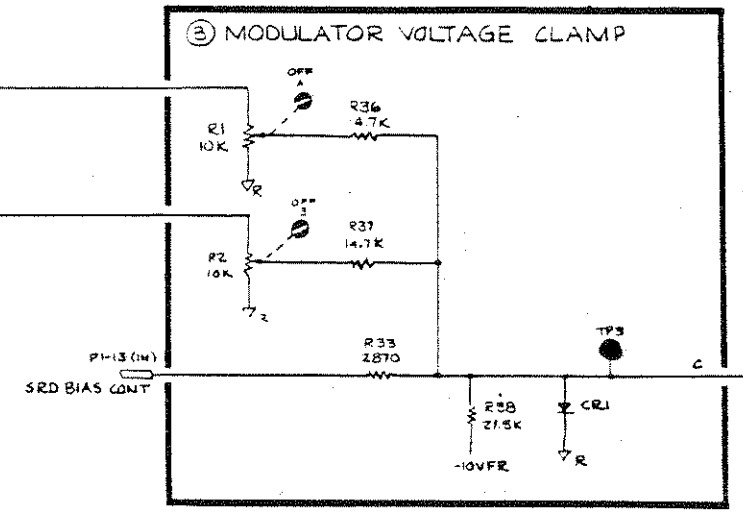


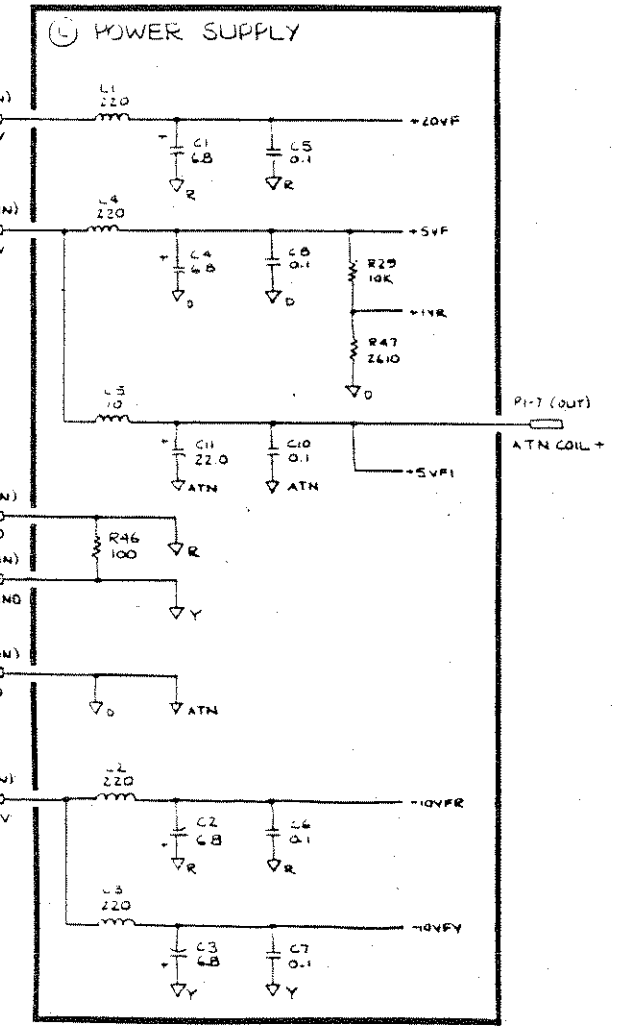
Figure 8-643. A24 Attenuator Driver/SRD Bias,
Component Location Diagram
8-365/8-366

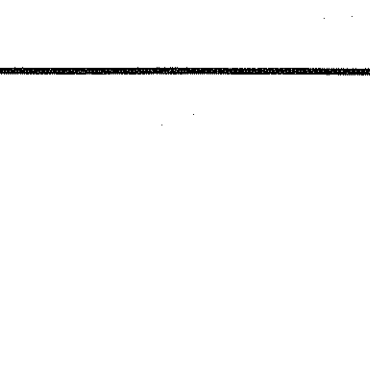
A24 ATTENUATOR DRIVER AND SRD BIAS (08340-60023)

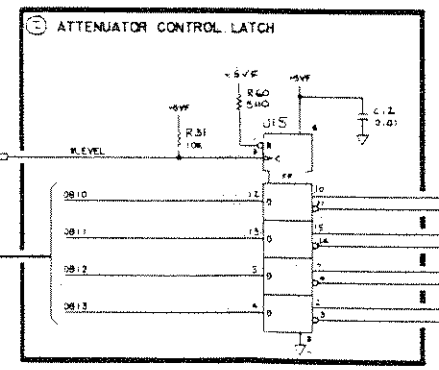


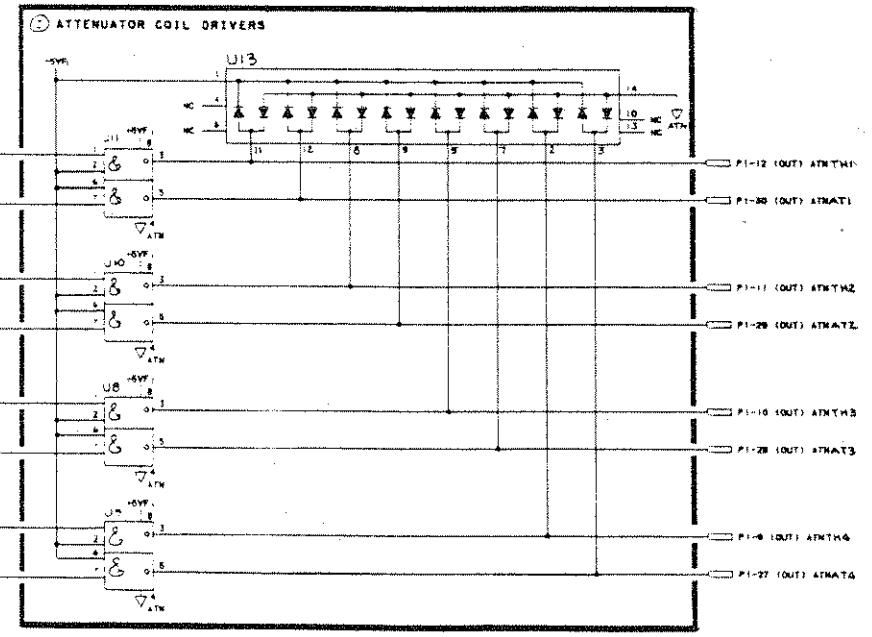




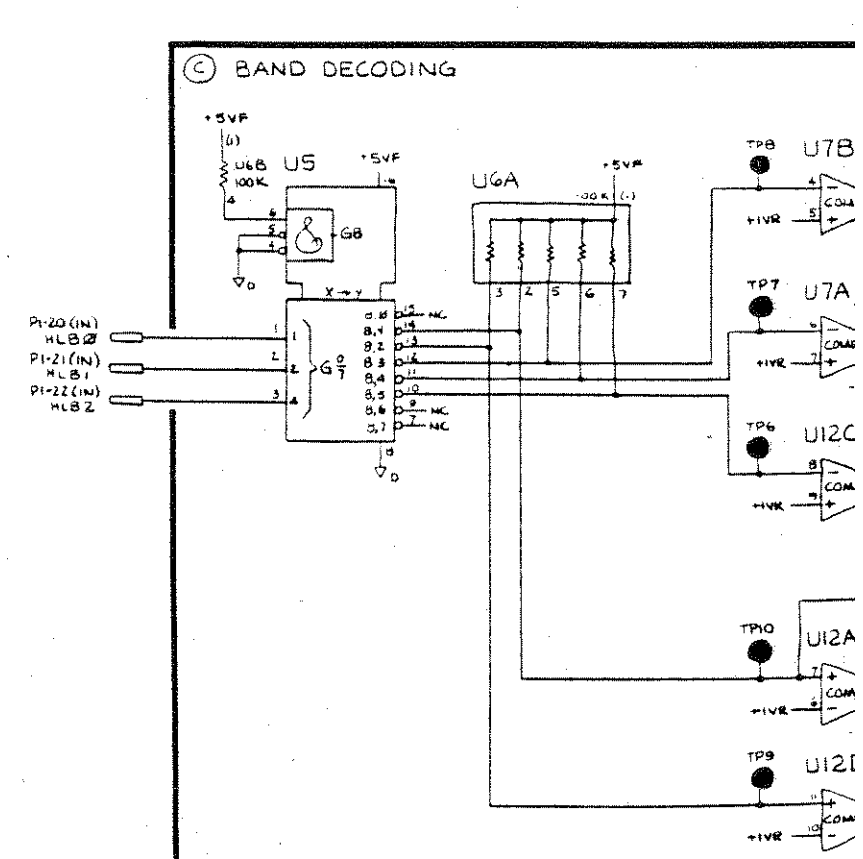








dB	ATTENUATOR SELECT			
	DB13	DB12	DB11	DB10
0	0	0	0	0
10	0	0	0	1
20	0	0	1	0
30	0	0	1	1
40	0	1	0	0
50	0	1	0	1
60	0	1	1	0
70	0	1	1	1



SERIAL PREFIX: A-2221-45 29 SEPT 82

TP4 TP5

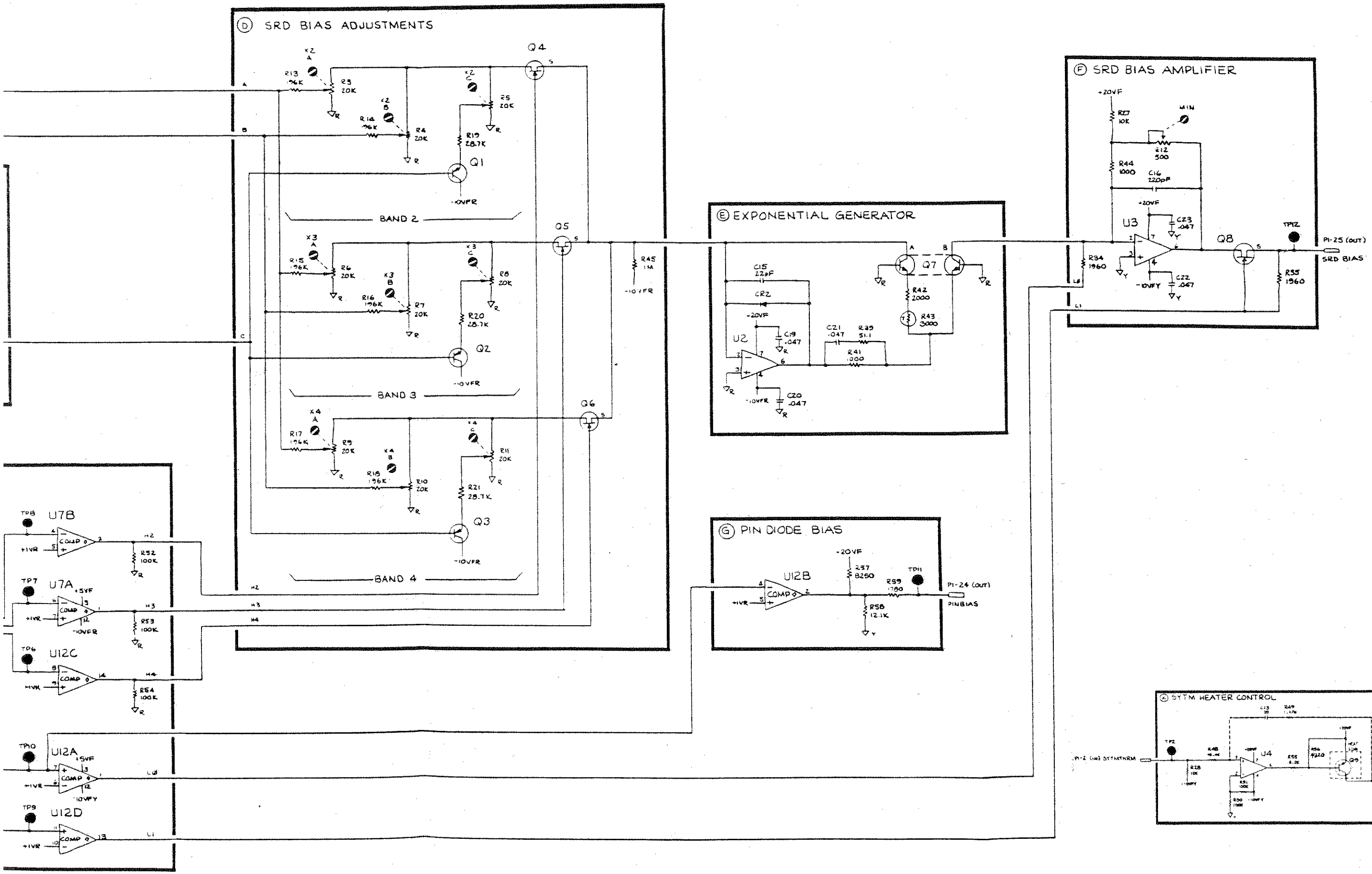


Figure 8-645. A24 Attenuator Driver/SRD Bias, Schematic Diagram

A25 ALC DETECTOR, CIRCUIT DESCRIPTION

Introduction

The A25 ALC Detector assembly processes the voltage from either internal or external detectors, producing an output voltage proportional to the RF power level. This voltage is then compared to a reference level voltage on A26 Linear Modulator Assembly, and the resulting error is used to drive RF modulators to control the RF leveling loop. Two ''log converters''; one for the internal detectors, another for external detectors or power meters, convert the detected RF voltage to a signal proportional to RF power in dBm. In addition, an amplifier buffers this voltage to be read by an ADC A27 on the Level Control board to display the front panel ''Power dBm'' function. Lastly, the reference level voltage is temperature-compensated on this assembly.

Internal Detector Log Converter A

The Internal Detector Log Converter receives the detected RF voltage and outputs a signal proportional to RF power level in dBm.

Crystal detectors characteristically exhibit two distinct regions of operation. At low power levels (less than 0 dBm), the detectors are in their ''square-law region''. The detected output voltage then varies with the square of the RF voltage. At high power levels (more than +10 dBm), the detected output voltage varies linearly with the RF voltage. The ''log'' function converts the detected RF voltage into a DC voltage proportional to RF power, but to track the detectors accurately through both regions requires halving the gain at low power levels. Alternately, the gain can be doubled at high power levels. The Log Converter is a ''dual-slope'' design that accomplishes this with a smooth transition between square-law and linear regions.

Figure 8-647A illustrates a simplied ''single-slope'' log converter. The ''log'' function is accomplished by Q6A using the transistor characteristic that collector current is the exponential of base-to-emitter voltage. U1 amplifies the detector voltage, driving the emitter of Q6A until the collector current sensed through R21 equals the input voltage. Q6A's emitter voltage is then the log of the input voltage, which passes through Q6B (wired as a diode) to the output.

To implement a ''dual-slope'' Log Converter, a second pair of transistors with bias current sources is added, as in Figure 8-647B. Bias currents Ib1 and Ib2 are constant and nearly equal. Q6A and Q6B still carry the logging current Iin; however, Q5A and Q5B now carry Ib1 and Ib2 in addition. For low power levels (square-law region), assume Iin << Ib1 and Io << Ib2. (Iin = Vin/R21) Then Q5A and Q5B are carrying essentially identical currents, and their base-to-emitter

voltages are identical. In effect, then, the emitter of Q6A is at the same voltage as the emitter of Q6B, and the circuit acts like the single-slope logger of Figure 8-647A. For high power levels (linear region), Iin >> Ibi. Now Q5A and Q6A both carry the same current Iin (Ibi can be ignored), and the base voltage of Q5A varies twice as much as the emitter of Q6A (both base-to-emitter junctions contribute to the logging function). Thus, the gain of the logger is doubled when the detectors are in their linear regions, and the Log Converter outputs a voltage proportional to RF power in dBm over a wide range of power levels encompassing both square-law and linear regions.

Actual Circuit Details: Q1 and Q2 (Block A) select the A12 Band 0 Detector or A11 Band 1-4 Detector when appropriate. U2D and U2C, through R33 ''L-20'' and R34 ''H-20'', add minute offsets in Band 0 and Band 1-4 respectively for to adjust low RF power levels. U1 and Q3 form a low-drift, high-gain DC amplifier to drive the logger. Q12, Q13, Q14, and Q15 for a high-speed differential AC amplifier to improve the loggers high-frequency response. Q4 sums the DC Amplifier and AC Amplifier to drive current through the logger. Q7 biases Q4. The logger consists of Q5 and Q6, and functions like the simplified ''dual-slope'' logger described in Figure 8-647B. R24 is added to compensate for bulk resistance in Q5A and Q6A at high currents. Q8 and Q9 provide the adjustable bias currents Ib1 and Ib2, respectively. U2B and U2A turn on the logger bias for Band 0 and Band 1-4 respectively. R38 ''L+10'' and R108 ''LOFS'' adjust the bias for Band 0; R39 ''H+10'' adjust the Band 1-4 bias. A thermistor mounted inside A12 Band 0 Detector changes the bias current Ib1 to improve temperature tracking. Q16 provides the bias current Io. In addition, Q16 serves to clamp the logger's negative excursions when pulse modulation turns the RF OFF. The clamp voltage is approximately -0.12 Vdc, but is caused to vary slightly with changes in power level, reference power level, and temperature to minimize recovery time.

X5 Amplifier B

Q17, Q18, Q19, and Q23 form a discrete differential amplifier to buffer the Log Converter's high-impedance output. In addition, the LVLCOR (level correction) signal from the A27 Level Control Assembly is summed together with the detected voltage.

Sample/Hold C

The Sample/Hold circuit ''remembers'' the detected RF level when the RF power is OFF during pulse modulation. Sampling switch Q25, holding capacitor C25, and buffer U8 are the key elements. Sampling switch Q25 is controlled by the A21 Pulse Modulator assembly through drivers Q30 and Q31. When Q25 goes open to ''hold'', some charge on C25 is lost through gate capacitance. C24 injects a charge into C25 to compensate for this charge loss, adjustable by R58 ''BAL''. The charge lost through Q25 during switching depends on the gate voltage excursion,

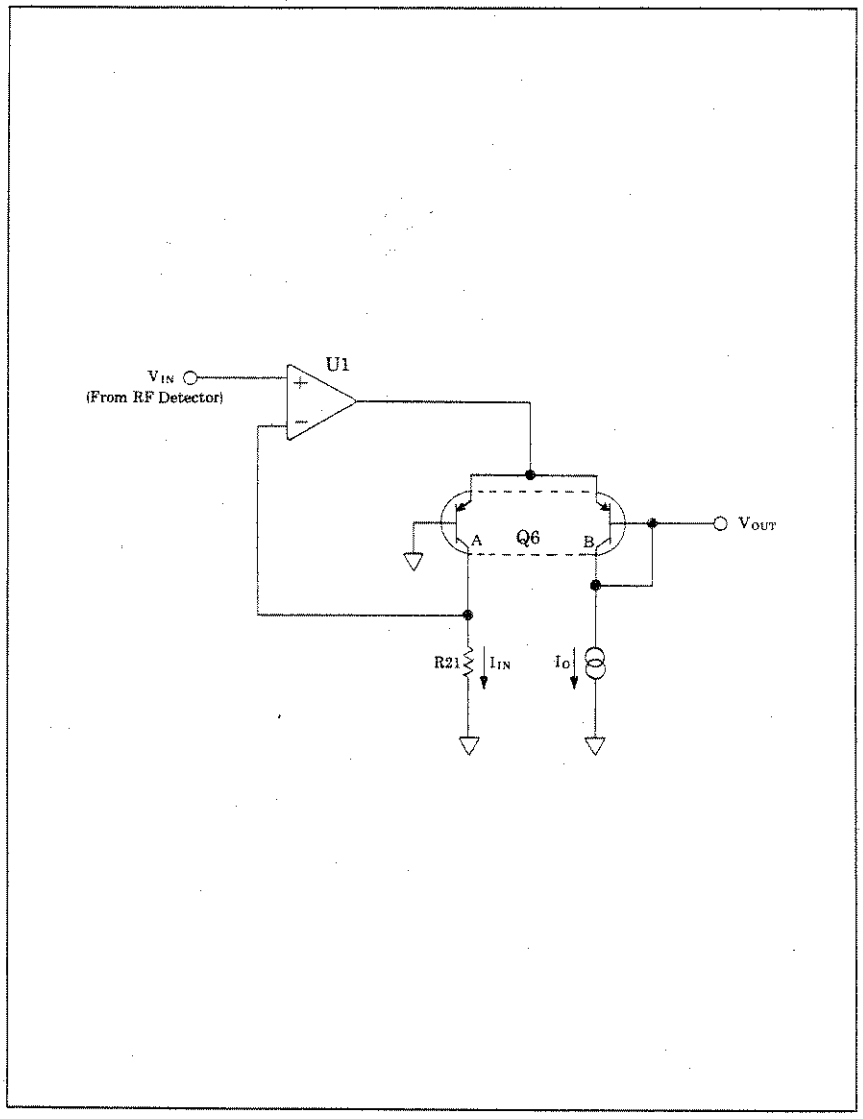


Figure 8-647A. Simplified Single-slope Log Converter Diagram

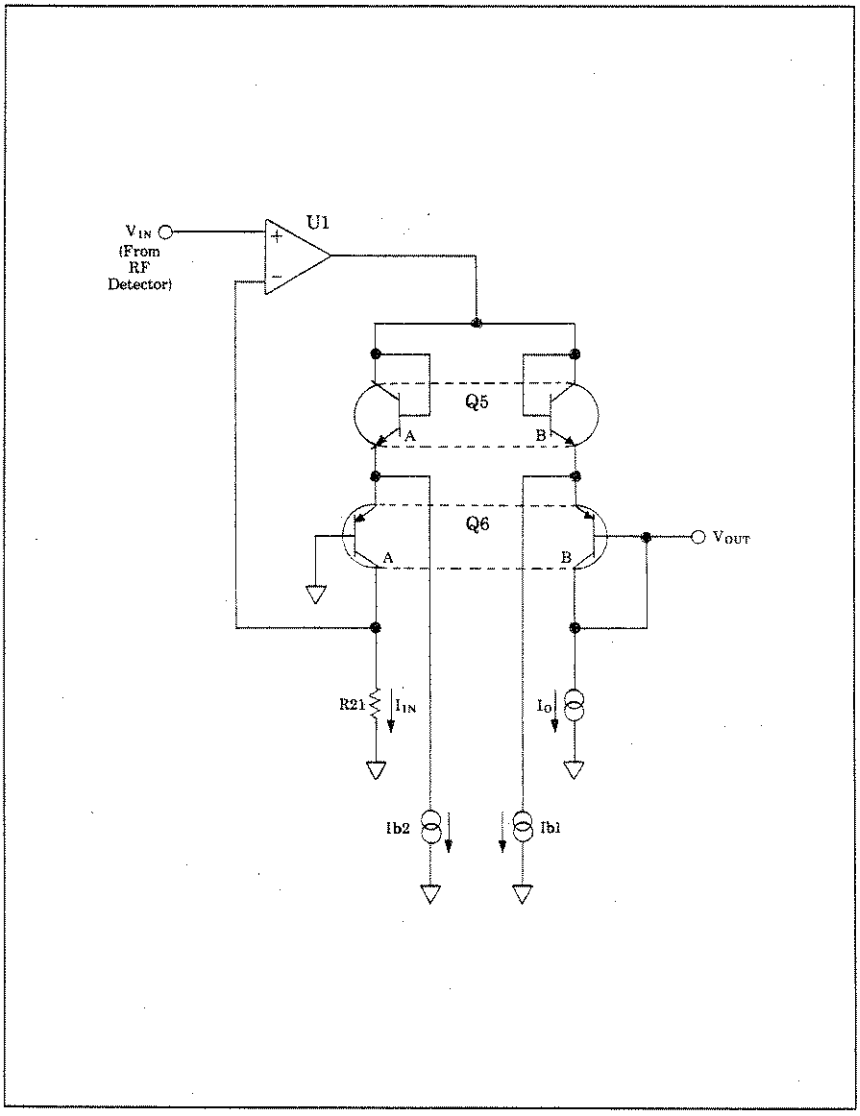


Figure 8-647B. Simplified Dual-slope Converter Diagram

which in turn depends on the sample/hold input voltage. Q24 monitors the output voltage and clamps the excusions of Q30 and Q31, so that the charge lost during switching is independent of power level. During bandswitching, the logger may produce negative transients large enough to accidentally turn ON Q25; CR4 and CR5 clamp these excursions. Note that R61 will keep Q25 ON if the A21 Pulse Modulator Assembly is removed.

Level Meter Amplifier D

Q20 and U4B buffer and filter the sample/hold voltage level. The amplifier has a voltage gain of Approximately 6.6, and a low-pass filter cutoff frequency of only 5Hz. Temperature-sensitive resistors R64 and R66 track the temperature drift of the logger and adjust the gain slightly. U5B buffers the signal to be read by the ADC on the A27 Level Control assembly. The microprocessor can then monitor the RF power level and display it on the Front Panel Power dBm display.

External Log Converter E

If the RF power level is monitored externally though the ''LEVELING EXT INPUT'', the External Detector Log Converter provides the logging function similar to the log converter in Block A. U10 and U6 form an ''absolute value converter'' to permit both positive and negative detectors to be used. U10 is a non-inverting amplifier with gain of 2.2, so when the ''EXT INPUT'' is positive, U10 pin 6 goes positive. This turns CR6 OFF, and U6 pin 6 will then go negative, turning CR9 ON and configuring U6 like an inverting amplifier to drive the logger through R86. When the ''EXT INPUT'' is negative, U10 pin 6 goes negative. This turns CR6 ON, causing U6 pin 6 to go positive and turn CR9 OFF. Thus, U6 is effectively removed from the circuit, and U10 drives the logger through R81, R85, and R86 directly. Resistor values are used to make the current to the logger the same for both positive and negative voltages. R80 ''EX-'' adjust the voltage offset of U10; R84 ''EX+'' adjust the voltage offset of U6.

U7 and Q22 form an inverting log converter. U7 drives the emitters of Q22A until the collector current equals the input current. (The input current may be driven by either U10 or U6.) Q22B is wired like a diode, and passes the base-to-emitter voltage out. Q21B provides bias current for Q22B; Q21A will clamp the logger's negative excursions to approximately -0.3 Vdc, and is normally turned OFF. R88 compensates for bulk resistance in Q22A at high logger currents.

Note that when external detectors are used, the Sample/Hold is not effective during pulse modulation. Furthermore, the Front Panel Power dBm display will continue to display the internally detected power level, not the externally detected power level.

Function Switches and External Detector Frequency Compensation F

U3 buffers the External Detector Log Converter, with a DC voltage gain of approximately 10. Open-collector drivers U9 and FET swtiches Q27 and Q28 select the internal or external detector signal, as appropriate, for use on the A26 Linear Modulator assembly. Q29 adjusts the frequency compensation for external meter leveling. The U9 open-collector FET drivers pull down to -10 Vdc to turn the FETs OFF, and float HIGH to turn the FETs ON. Refer to Table 8-647A for a function select truth table.

Level Reference Temperature Compensation G

To compensate for gain drift in the log converters, the reference voltage is made to change with temperature. This is accomplished by inverting amplifier U4A which has a temperature-dependent feedback resistor R101. The temperature-compensated reference voltage (TCREF) goes to the A26 Linear Modulator board where it is summed with AM and marker inputs, then compared to the output of the A25 ALC Detector board.

Power Supply H

LC filtering removes noise from the +20VF and -10VF lines for use on the A25 ALC Detector Assembly. Additional RC filtering keeps +20VL and -10VL extra clean for use in the internal logger. The +1.5VF is the TTL reference voltage for the comparators.

Table 8-647A. Function Select Truth Table

Leveling Mode		Q27	Q28	Q29
Internal		ON	OFF	OFF
External	Crystal Detector	OFF	ON	OFF
	Power Meter	OFF	ON	ON
Unleveled (Shift Meter)		OFF	OFF	OFF

Table 647A. Function Select Truth Table

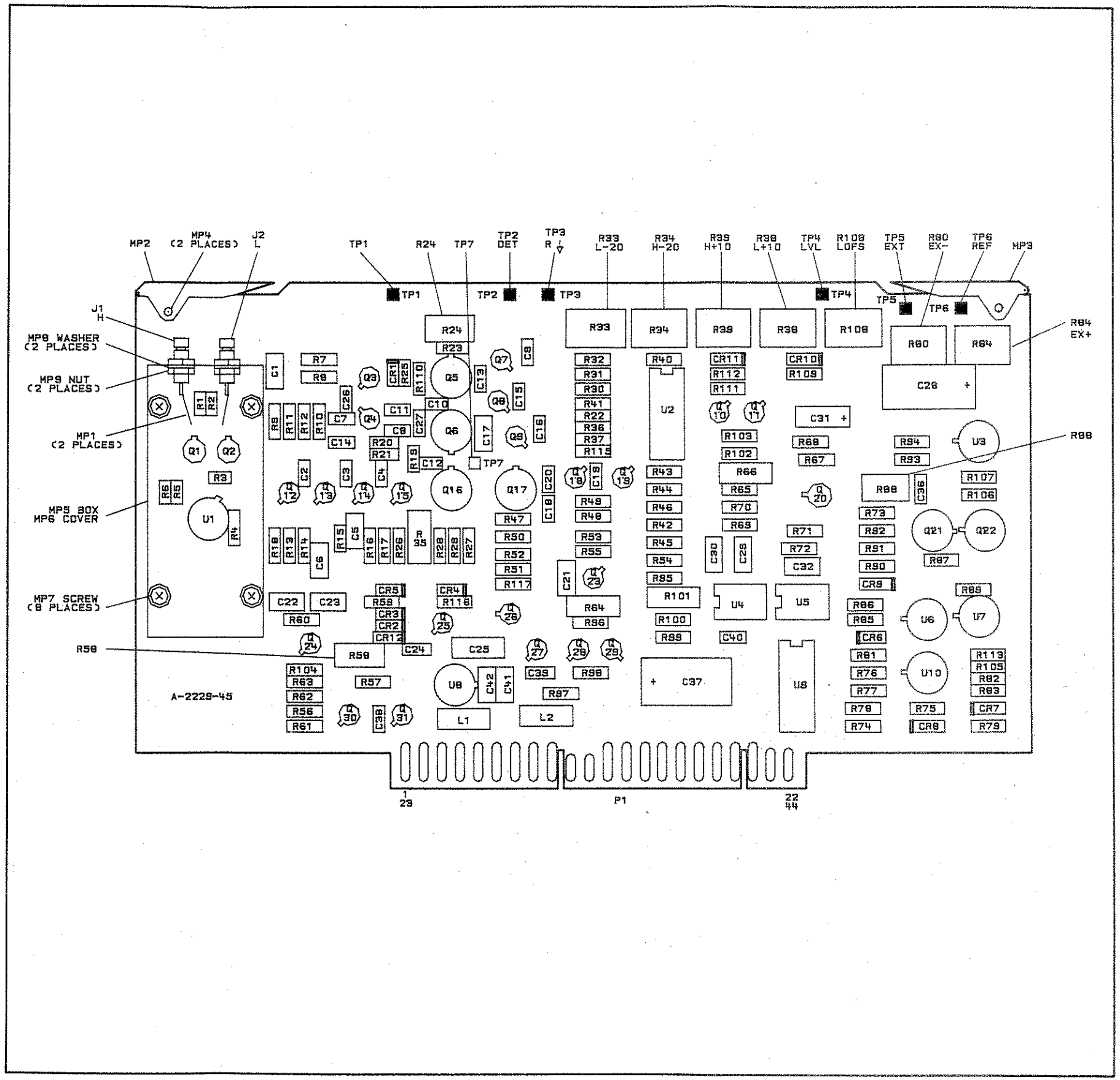


Figure 8-649. A25 ALC Detector, Component Location Diagram

Ⓐ INTERNAL DETECTOR LOG CONVERTER

SHIELD BOX

BAND 1-4 DETECTOR INPUT (A11) H

BAND 0 DETECTOR INPUT (A12) L

J1 J2 Q1 Q2 R1 100K R22 100K

U1 +20VL -10VL

TP1

DC AMPLIFIER

AC AMPLIFIER

R8 464 C26 1000pF Q3 CR1 C7 .047 Q4

R11 1000 R12 1000 R10 750 C8 47pF

Q12 Q13 Q14 Q15 R3 100 R4 1M R9 1000 C2 .047 C3 15pF C4 .047 R19 100

R13 1100 R15 75 C5 1.0 R17 1100 R14 4220 R16 4220 R20 75

Q7 R22 1960 C9 .01 R

LOGGER

R110 100K R23 5.62 R24 10 CW +20 C13 1000pF

Q5 C10 1000pF Q6 C27 22pF C14 .047 R21 75

TP7 0V AT 0dBm +6mV/dB

LVLCOR

U2C U2D COMP +1.5VF

P1-37 (IN) LHET

R34 20K H-20 R30 61.9K R32 19.6K R33 20K L-20 R31 19.6K R5 14.7K R6 100 SHIELD BOX

LOGGER BIAS

Q8 Q9 R41 6190 C15 .01 C17 0.1 R

Q16 Q26 R26 56.2K R35 320 R27 681 R117 7500 R116 21.5K C12 100pF R28 38.3K R29 196

LOGGER CLAMP

P/O A12 BAND 0 DETECTOR

THERM1 20K THERM2

R115 5110 R36* 5110 R40 619 C16 .01

L+10 H+10 R38 2000 R39 2000 R109* 1960 R108 5000 LGFS R37* 4220

CR10 CR11

U2B U2A COMP Q11 Q10 R111 10K R112 10K

Ⓑ X5 AMPLIFIER

+20VF R42 5000 R43 1330 R44 5000 Q18 Q19 C19 4.7pF R45 3480 R46 3160 -10VF

Q17 R47 147 C18 10pF R48 5110 R49 5110 +800mV/dB

P1-14 (IN) LVLCOR

Ⓗ POWER SUPPLY

P1-5, 27 (IN) +20V L1 4.7 R7 19.6 C41 1.0 C1 1.0 +20VL +20VF +1.5VF

R102 17.8K R103 1470

TP3 A6ND P1-12, 34 (IN) A6ND R25 10 C11* 1000pF NOTE 3

P1-7, 29 (IN) -10V L2 4.7 C42 1.0 R104 1210 R18 19.6 C6 1.0 -10VF -10VL

Ⓔ EXTERNAL DETECTOR I

U10 +20VF CR7 CR8 -10VF

P1-44 (IN) EXDET R74 1000 R75 1M

P1-43 (IN) EXDETR R73 10 R76 4640

R77 3830 R79 196K R78 10 R80 20K R84 20K EX- EX+ CW

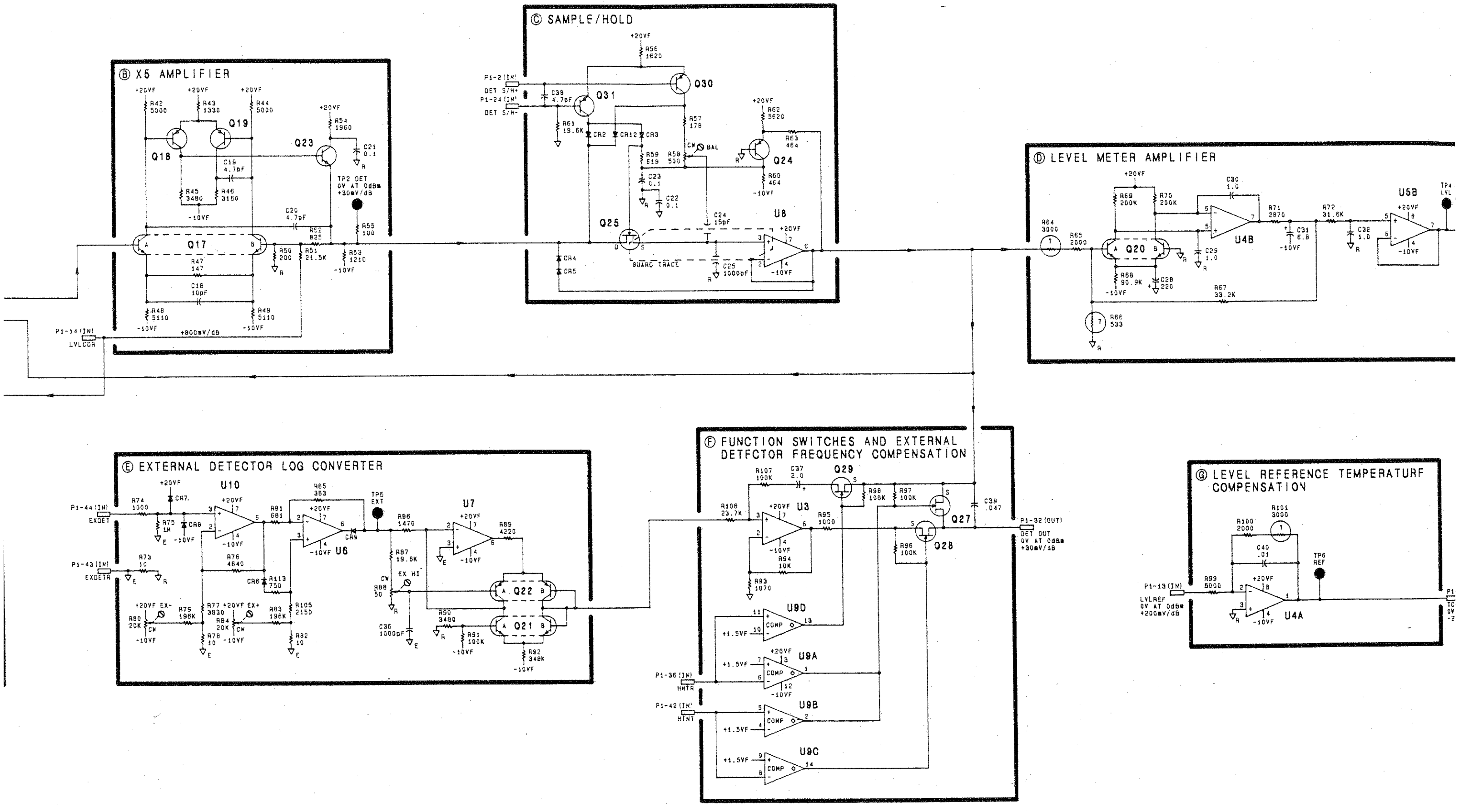


Figure 8-651. A25 ALC

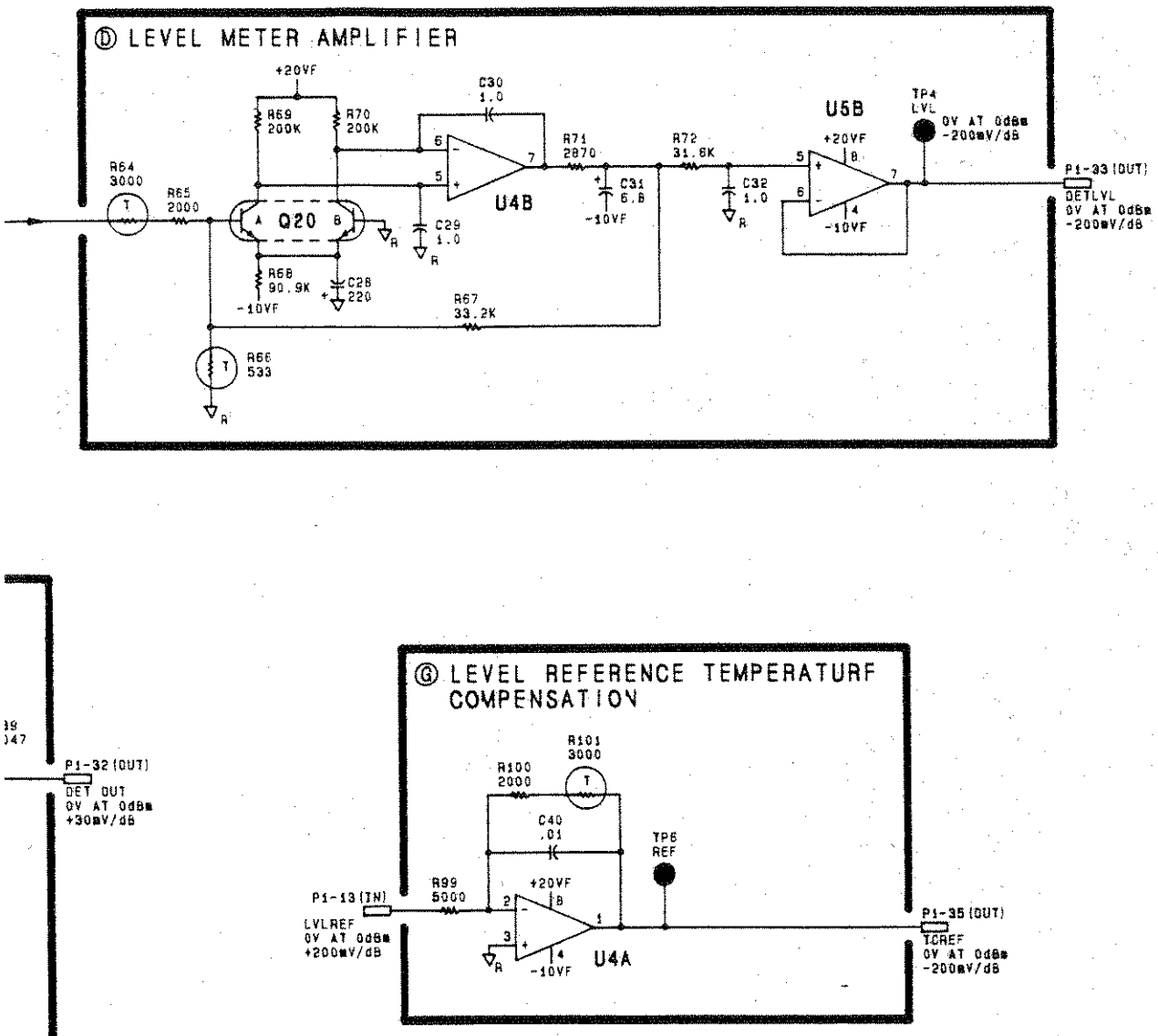


Figure 8-651. A25 ALC Detector, Schematic Diagram

A26 LINEAR MODULATOR, CIRCUIT DESCRIPTION

Introduction

The A26 Linear Modulator assembly compares the detected RF power level against the level reference voltage, and drives the RF modulators to correct any errors. This closes the ALC loop and levels the RF power. The amplitude modulation (AM) input is logged and added to the level reference on this assembly.

External AM Log Converter A

U12 buffers the front panel ''AM MODULATION INPUT'' with approximately unity gain. U1 and Q24 form the log converter. (See Figure 8-653A for a simplified diagram of the External AM Log Converter.) U12 drives a current through R23 to U1; a constant bias current Ib (through R26) establishes the operating point of the logger. U1's output will drive the emitter of Q24A until its collector current equals the total input current. The base-to-emitter voltage is then logarithmically related to the input voltage. This voltage is sensed through Q24B to the output. U2 buffers the log converter's high output impedance, and has a voltage gain of about 10. FETs Q23 and Q1 switch out the log converter when AM is not selected.

ALC Loop Integrator B

The ALC loop summing node is at the source of FET Q16. At this point, the detected RF power level voltage (DETOUT) is summed with the reference power level voltage (TCREF). When the loop is closed and leveled, these signals should be equal and opposite, thus perfectly cancelling. If they do not cancel, the error current is integrated by U8 and changes the RF modulation level to correct the power level. FET Q9 can be closed to double the TCREF sensitivity under the open-loop condition. The marker pulses (HMRKR) and logged external AM (if enabled) are also added to the summing node.

U8 is the main ALC amplifier, forming an integrator with capacitor C6 (ALC Loop BW = 100kHz). C15 is switched in parallel with C6 by FET Q20 in any externally leveled mode (ALC Loop BW = 20kHz). Under a variety of conditions, C7 is also connected in parallel with C6 (ALC Loop BW = 7 kHz; see Table 8-653A). Q17 clamps the negative voltage excursions of U8 to about -3.9 V when the loop goes unleveled; likewise, Q18 clamps the positive excursions to about +0.5 V. U11B and Q25 alter the bias on these clamps when HRFON goes low to turn the RF power OFF, clamping the MOD LVL voltage at about -3.0. When external power meter leveling is selected, FET switch Q30 is closed to put C23 across Q25's control line. This makes the ''turn-on'' time at bandswitches or

beginning of sweep very slow and avoids ALC overshoot due to slow power meter response times. (Leveled ALC Loop BW is not affected.) Q10 is normally OFF, but can be turned ON to shunt R17 across the integrating capacitors C6, C7, and C15. This makes U8 an inverting amplifier instead of an integrator for the ''open-loop'' conditions.

Overmodulation And Unleveled Detectors C

The MOD LVL voltage will remain within certain bounds when the RF power is leveled. If MOD LVL exceeds these bounds, comparators detect the condition and send the information to the microprocessor. Q27 and U14 detect excessive amplitude modulation. When MOD LVL falls below about -3.6 V, Q27 turns ON, trips U14, and sends LOMD to A27 for the microprocessor to read. Likewise, Q26 and U13 detect the MOD LVL when the RF modulators are no longer attenuating and the RF power is unleveled. If LVL MOD rises above about +0.2 V, Q26 will turn ON and trigger U13 to send LUNLVL to A27. Both functions are disabled by Q28 when HCMPEN (High = Comparators Enable) goes LOW.

Modulator Driver G

The ALC loop gain is adjustable for each band separately. Q2, Q3, Q4, Q5, and Q6 select the MOD LVL to pass through an adjustment for Band 0 through 4 respectively. U7 buffers this voltage for Bands 2-4 and sends it to the A24 assembly for use in biasing the Step Recovery Diode in the A13 SYTM. Each of the five adjustments drives the emitter of Q15 one at a time. Q15 forms a common-base current summing node. Q7 and Q8 form an ''exponential current mirror'' to drive current through the RF modulators.

The exponential function is desirable to linearize the RF modulators' attenuation characteristics. (See Figure 8-653B.) The RF attenuation of the modulator is a very non-linear function of drive current. If plotted on log-log paper, however, the plot is straight over the high current end of its range. Therefore, converting the MOD LVL voltage to an exponential current would best fit the modulators' characteristics at high attenuation levels. To track the modulator curve better at low attenuation, simply subtracting a fixed current from the exponential current mirror's output will ''bend'' the modulation curve on log-log paper. This gives the desired result: RF attenuation in dB is proportional to the MOD LVL voltage. In Bands 2-4, non-linearities in the power transfer characteristics of the A13 SYTM require additional modulator drive shaping.

R54 and CR9 bias Q15's emitter at about 0 V. Q15 is a common-base current summing node: the collector current is the same as the emitter current. Q8, with R85 and R55, form an exponential

current mirror: current through Q8A causes a voltage drop across R85 and R55. This causes Q8B's base-to-emitter voltage to change linearly, causing Q8B's collector current to change exponentially. Q7 is added in a Darlington configuration to buffer Q8B. R86, R87, R88 ''MO'' (Modulator Offset), and R44 sink current to offset the current subtracted later, as mentioned above. Q14 sinks still more offset current for Bands 2-4 only.

Modulator Bandswitches D

FET swtiches Q21 and Q22 select either the Band 0 (P/O A8) or Band 1-4 (P/O A16) RF modulators to be driver by the Modulator Driver. In Band 0, LB0 goes low, causing U11D pin 14 to go to ground to turn Q21 ON. At the same time, U11C pin 8 goes high to turn Q22 OFF. Note that U11C also biases the high band switch (P/O A16) OFF in Band 0. (Refer to RF Schematic.) In Bands 1-4, the situation is reversed: Q21 is OFF, and Q22 is ON. R62 sinks a fixed current from the exponential current mirror in Band 0, as described above. In Band 1, R61 sinks this current; in Bands 2-4, R60 in parallel with R61 sinks the bias current.

Bandswitch Drivers F

U4 decodes the band information from HLB0, HLB1, and HLB2. Each output goes LOW for the selected band, causing the output of each respective comparator to go HIGH for the selected band. U10A senses the Band 0 and Band 1 lines, but actually drives U11A pin 1 HIGH during Bands 2-4 to alter the modulator bias for the multiplying bands.

ALC Loop Function Switch Drivers E

U15 latchs digital information from the microprocessor to control the major ALC functions. Many of U15's outputs are used on other boards in the ALC loop. HMTR and HINT determine the primary leveling mode. These two lines, with decoders U10C and U10B, drive comparators to control the Main ALC Amplifier. See Table 8-653B for their functions. The other lines and comparators control functions for loop bandwidth, enable amplitude modulation, and enable the overmod/unleveled comparators. U9C controls the A12 Band 0 Detector bandwidth.

Power Supply H

The power supply filtering consists of ordinary LC filters. R80 and R81 generate the +1.5VF reference voltage for TTL comparators.

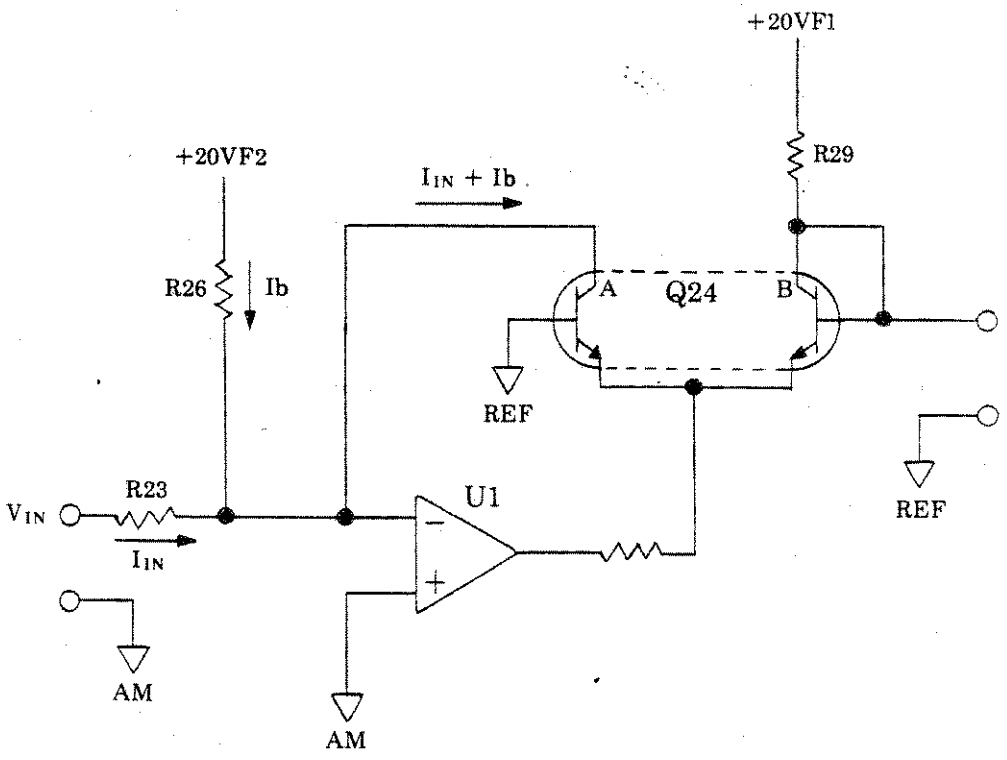
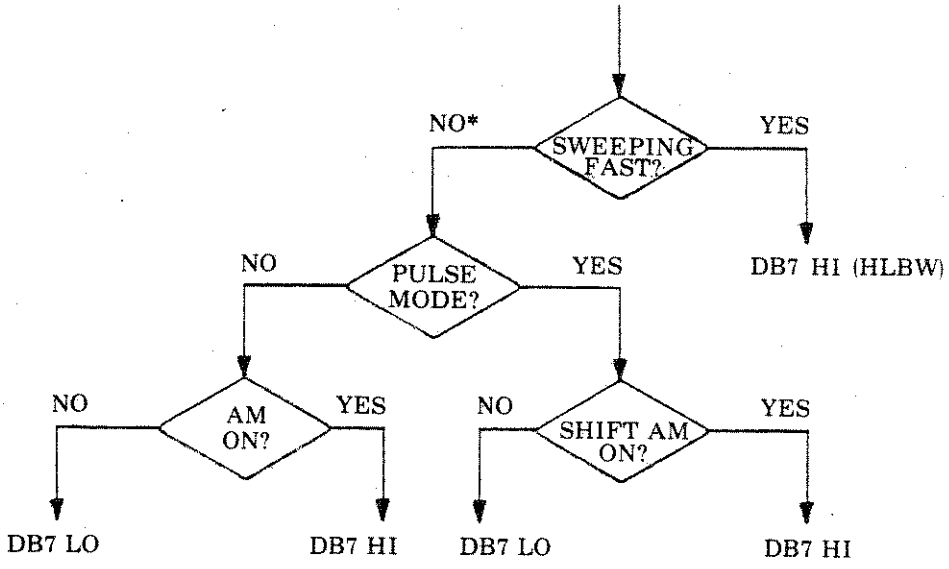


Figure 8-653A. External AM Log Converter, Simplified Diagram



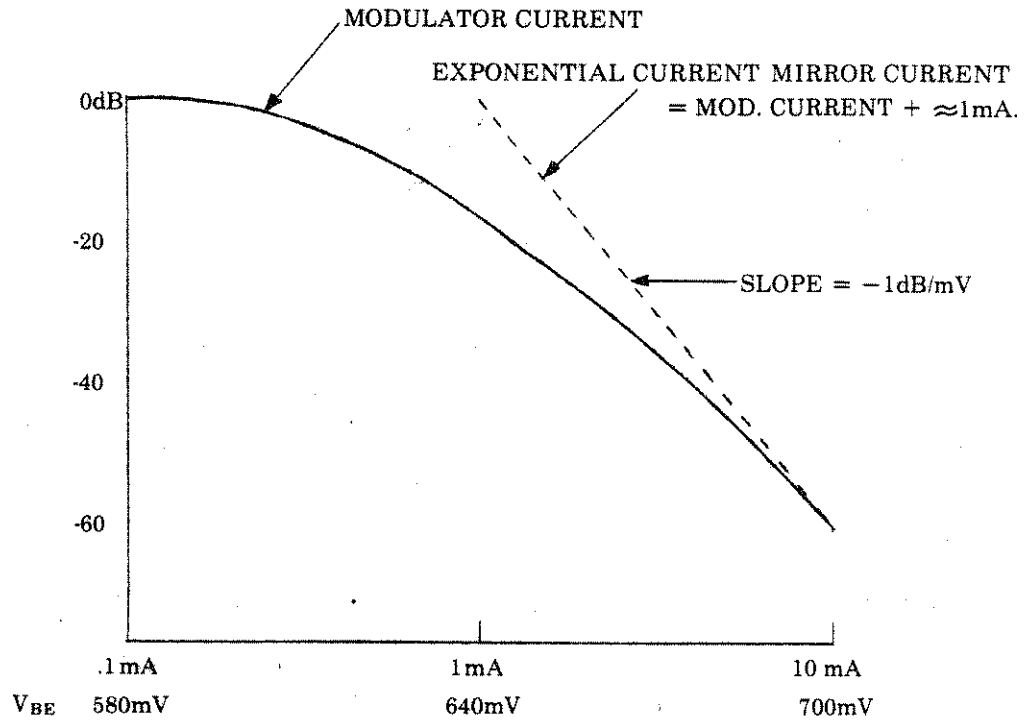
FAST SWEEP: <5 SEC.

* INCLUDES MANUAL & CW

SHIFT AM ACTIVATES AM

TURNING AM OFF DE-ACTIVATES SHIFT AM

Table 8-653A. HLBW Algorithm



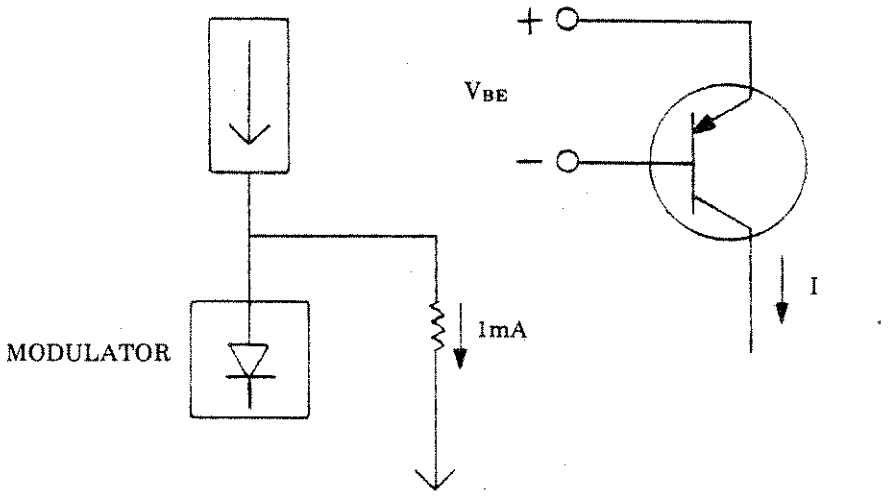


Figure 8-653B. Modulator Characteristic

Table 8-653B. HMTR and HINT Functions

HMTR	HINT	
	Low = 0	**High = 1**
High = 1	External Power Leveling	"Open-Loop"
Low = 0	External Crystal Leveling	Internal Leveling

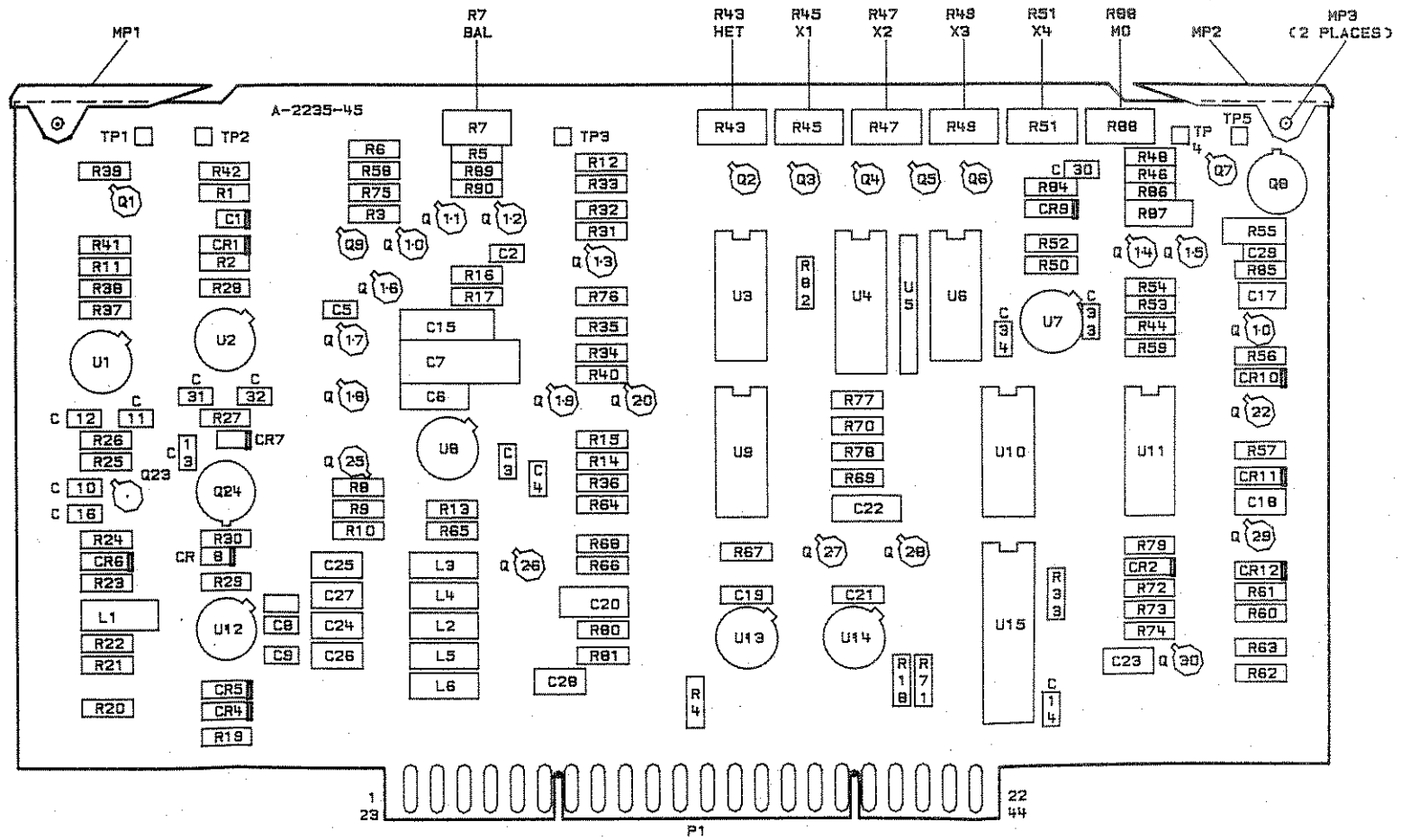
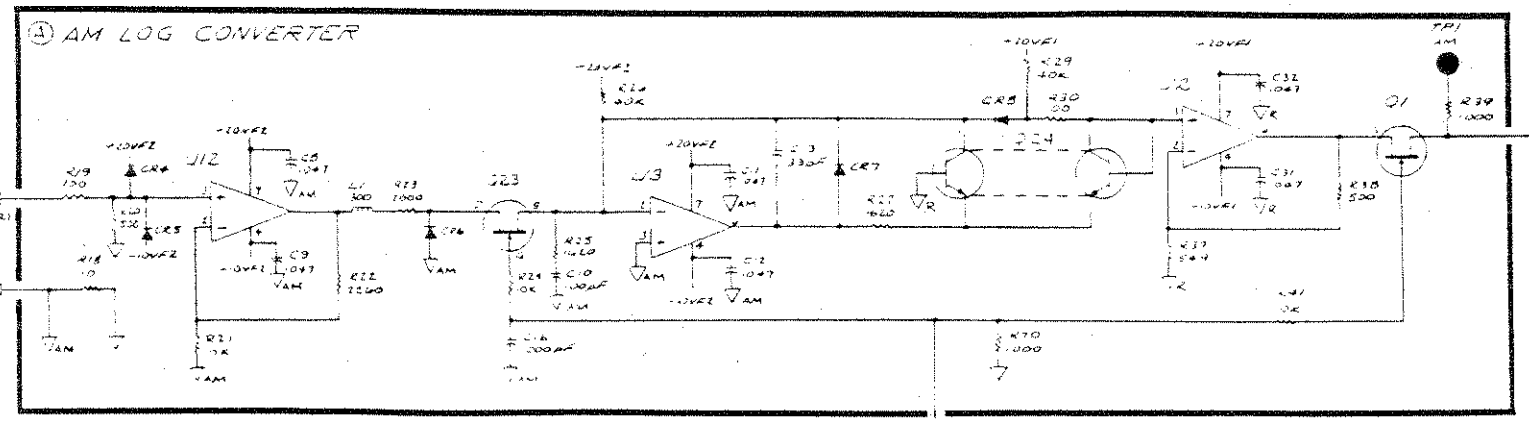
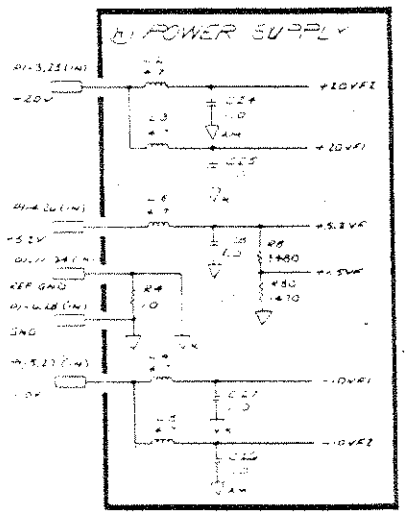


Figure 8-655. A26 ALC Modulator,
Component Location Diagram

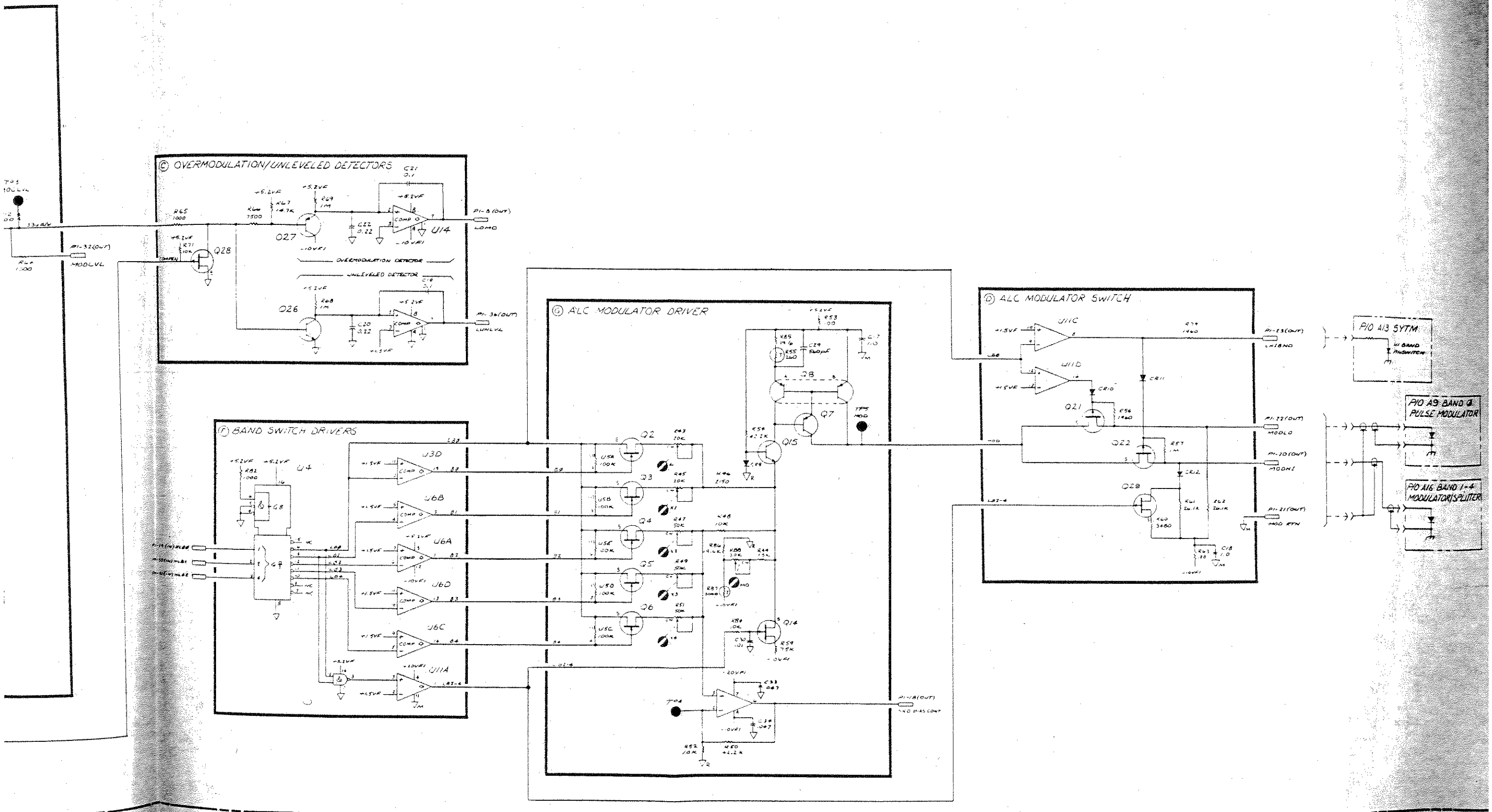
A26 ALC MODULATOR BOARD
08340-60021





SERIAL PREFIX: A-2138-45 5 NOV 82

TP1 TP2 TP3


TP3
10 LVL
33 dB/V
P1-32(OUT)
MODLVL
R65 1000
R66 7500
R67 14.7K
R69 1M
C21 .1
+6.2VF
+5.2VF
+8.2VF
Q27
Q28
U14
C22 0.22
-10VF1
P1-8(OUT)
LOMO
OVERMODULATION DETECTOR
UNLEVELED DETECTOR
R68 1M
C19 .1
Q26
C20 0.22
P1-36(OUT)
UNLVL
+13.5VF
C OVERMODULATION/UNLEVELED DETECTORS
F BAND SWITCH DRIVERS
U4
R61 1000
G8
U3D
U6B
U6A
U6D
U6C
U11A
G9
P1-15(OUT) HLB8
P1-30(OUT) HLB1
P1-29(OUT) HLB2
G BLC MODULATOR DRIVER
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q15
Q16
R43 10K
R45 10K
R47 50K
R48 10K
R49 50K
R51 50K
R53 100
R55 1K60
C29 560pF
C27 1.0
R56 42.2K
C28
R57 2.50
R58 33K
R59 75K
C30 .01
C31 .047
C32 .047
R60 +1.2K
R52 10K
P1-7(A)(OUT)
MOD BIAS CONT
D ALC MODULATOR SWITCH
U11C
U11D
R54 1K60
P1-23(OUT)
LMBAND
CR10
CR11
Q21
R56 1K60
P1-22(OUT)
MODLO
Q22
R57 1M
P1-10(OUT)
MODHI
CR12
Q28
R61 2W 1K
R62 2W 1K
R60 3480
P1-21(OUT)
MOD RTN
C18 1.0
P/O A13 SYTM
W BAND PINSWITCH
P/O A9 BAND 4 PULSE MODULATOR
P/O A16 BAND 1-4 MODULATOR/SPLITTER

Figure

NOTES:

1. REFER TO FIGURE 8- FOR DETAILED SCHEMATIC DIAGRAM SYMBOLOGY NOTES.
2. RESISTANCE VALUES SHOWN ARE IN OHMS, CAPACITANCE IN MICROFARADS, AND INDUCTANCE IN MICROHENRIES UNLESS OTHERWISE NOTED.

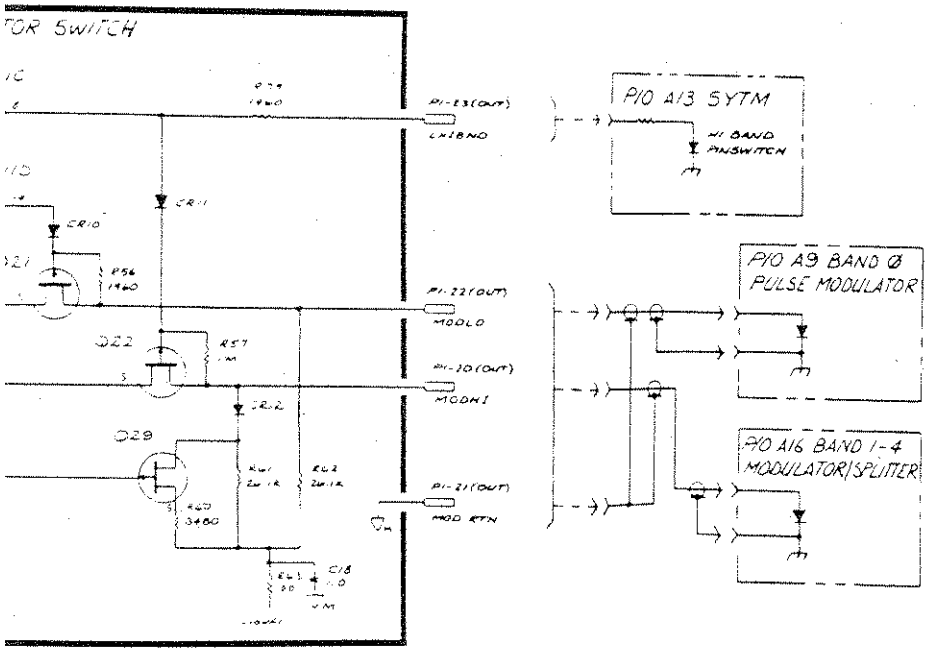


Figure 8-657. A26 Modulator, Schematic Diagram

A27 LEVEL CONTROL ASSEMBLY, CIRCUIT DESCRIPTION

Introduction

ADC Input Multiplexer A

The purpose of the ADC input multiplexer is to allow the processor to select which analog input line the ADC will convert to Digital information for use by the processor.

As discussed under Block E, AMUX0,1,2 are latched off the instrument data buss and determine which channel is selected. The output of the MUX (U25 pin 8) is connected to the summing node of an op amp. The buffer amp allows each channel to have a different gain and offset.

Channel 0 (U25 pin 4) is bipolar with a gain of 1 which will yield a full scale input range of ±5.0 volts. Channel 0 is the DET LVL input from the Detector board and is corrected to accurately represent the actual output power of the 8340A when this voltage is valid. The scale factor of this voltage is -0.2 V/dB or ± 25 dB fullscale.

Channels 1 thru 5 (U25 pins 5,6,7,12 & 11) are voltages that can be used by the processor to determine if major portions of the instrument are functioning correctly. Resistors R61 thru R64 are used to sum an offset current into the buffer amplifier (U18A pin 2) to offset its output (U18A pin 1) to -5 volts. This allows the measured voltage to vary from 0 to -10 volts while the ADC sees -5 to +5 volts. Channel 6 (U25 pin 10) is scaled to allow -3.53 to +2.47 volts input. MOD LVL is connected to this input and represents the amount of excess power that is available above what is being asked for by the ALC. If the SYTM is peaked by the processor so that more power is available, this voltage will change proportionately and if less power is available this voltage will change in the opposite direction. This input is required to provide feedback to the instrument processor for the auto-peaking and auto-tracking functions.

Channel 7 (U25 pin 9) will allow ±5 volt signals and is connected to TP 16 on the Level Control board. This input is used during testing of the ADC.

ADC Window Comparitor B

Since the ADC clock must not run when the voltage into the ADC is not changing, an external window comparitor in addition to the window comparitor that resides inside the Test ADC senses when the ADC clock should be turned on to allow the ADC to convert. The summing node of the current DAC inside the Test ADC and the

input current through R43 is sensed by the widow comparitor circuit. Whenever the input current does not match the current output from the ADC, an offset voltage proportional to the error between the DAC current and the input current exists. Both the internal window comparitor and the external window comparitor sense this voltage. The external comparitor is set to trigger when this voltage exceeds approximately ±1 LSB of the ADC. This window comparitor then starts a conversion. In this way the ADC clock can be turned off until the input voltage changes by more than approx. 2 LSB max.

U7 is an OP-07, a very low offset op-amp, which has been connected to provide a gain of approximately 19-20. Its purpose is to provide a larger voltage, representing one LSB to the comparitors. U7 must have an input offset voltage which is much lower than the comparitor's for this approach to help.

The filter formed by R46 and C38 prevents transients or noise generated by the clock circuit from triggering the comparitors when the voltage is within the window.

U2 and U3 form the window comparitor. R47 and R48 set U2 output HIGH until the (-) input (U2 pin 3) exceeds 75 mV. R49 and R60 set U3 output HIGH (U3 pin 7) until the + input (U3 pin 2 is less than -75 mV. C39 and C40 provide noise filtering. Bothe U2 and U3 are open collector output comparitors so R50 is provided to pull up this signal to 5 volts. This open collector line is called LOW Outside Window (TP 5).

Test ADC C

The purpose of the Test ADC is to provide the power level meter function during External Leveling, during AM to detect DC in the AM jack, during pulse operation and when ever an unleveled condition occures so the actual output power can be determined.

The requirements for the A/D Converter system are quite restrictive. First it must be 10 Bits. Second, it must be able to handle slowly increasing or decreasing input voltages. Third, it must not have a freerunning clock which could cause output spurs during CW operation. This third requirement imposes the restriction that the clock circuit and therefore the conversion should only be activated when a change in input voltage occurs. Forth this circuit must be able to be disabled by the main processor or the ALC circuitry at times when no conversion is necessary or when the input voltage is not valid. The processor must also be able to override the ALC's conversion holdoff if necessary.

The Tracking Analog to Digital Converter (U11) contains a D to A

converter and reference amplifier, an up/down counter, a window comparitor to control the up/down counter and data latches to store conversion data. A precision resistor (R17) is connected to the precision 10.00 V reference and to the converters Iref and Ref Amp + terminals (U11 pins 5 & 9). The Iref terminal connected to the reference current resistor (R17) is held at ground by the reference amplifiers input (U11 pin 5). The reference current is simply Vref/R17=1 mA. This reference current is multiplied by four in the DAC and then is divided appropriately according to the digital output of the internal 10 bit up/down counter. Iout of the DAC (U11 pin 10) is a current going into the A/D converter (U11 pin 11) and is summed into a 1 Kohm resistor along with an offset current of 2 mA thru R18 (10.00V/R18) and the input current determined by R43 (Vin/ 2.5 Kohm). This summing node is connected to the comparitor input (U11 pin 11) which compares this voltage to reference ground. Since this summing node is held at ground (via digital feed- back), the algebraic sum of the currents entering and leaving this node must equal zero. If the currents entering this node are slightly greater than the currents leaving the node the internal window comparitor will signal the up/down counter to count up. This will in turn increase the current sinking output of the DAC (Iout U11 pin 10) until it sinks just enough more current to compensate for the excess current entering the node. The reverse is true also, the window comparitor,up/down counter and DAC will compensate for a deficiency of current at the summing node by decreasing the amount of current sunk by Iout. The digital value contained in the up/down counter, when the currents at the summing node are in equilibrium, is the digital representation of the current entering the node thru R43. The offset current summed into the summing node thru R18 forces the digital value to the DAC (and digital ouputs) to be mid range when no current is flowing in the input resistor (R43). This allows a bi-polar input voltage at R43 so that both positive and negative voltages can be digitized. Iout (U11 pin 10) can be in the range from -0 mA to -4(1023/1024) mA and we have +2 mA summed in through R18 so the acceptable range of input currents thru R43 is -2 mA to +2(511/512) mA. This implies that input voltage range at R43 is -5V to +5V(511/512). -5 volts will yield a digital value of 0, 0 volts will yield 512, and +5(511/512) will yield 1023.

The digital outputs of the internal up/down counter go into transparent latches/output buffers. Whenever the Data Hold line (U11 pin 28) is HIGH, the digital information appears at the outputs (U11 pins 18 thru 27). If the Data Hold line is brought LOW, the information present at the DAC and up/down counters at that instant will be frozen in the output latch/buffers. Since the outputs are always enabled, the digital information appears directly at the inputs to two 74LS367 buss buffers (U12 & U15). When the main processor is ready for the ADC data it causes the

RLEVEL strobe to go LOW which enables the outputs of these buss buffers (U12 & U15 pins 1 & 15) and places the ADC data on the instrument data buss to be read by the instrument processor. This RLEVEL strobe is also connected to the Transfer line on the ADC (U11 pin 28) so that the information in the ADC latches cannot be changed while it is being read. The ADC requires that the transfer line cannot be brought LOW for 150 nS after the rising edge of the ADC clock to allow for settling of the counter outputs. Due to the asyncronous nature of the ADC clock and the RLEVEL strobe, the above restriction means that the ADC clock cannot be allowed to run while the ADC is being read.

Attenuator Installed Sensing

A pulled up line that is grounded by the installation of the attenuator is connected to the input of DB 10 of the ADC data output buffers (U15 pin 10). This bit will be read any time the processor does a read level operation. This info is used to determine if the attenuator has been installed.

ADC Conversion Complete Timer SRQ Latch D

The function of the converson complete timer is to allow the clock to run for 8 clock pulses after the widow comparitor has signaled that the ADC has converted the input voltage to within -1 LSB of the actual value. This will allow the ADC sufficient time to convert the input voltage down to within $\pm$0.5 LSB before its clock is stopped. (Assuming the input voltage is not changing.)

The output of the window comparitor (Low Outside Window) is invereted by U26C which drives Low Enable of a LS169 counter (U1 pin 7). This counter is enabled to count up when the voltage being converted is inside the window. After 8 counts the carry out (U1 pin 15) goes low which does a parallel load (U1 pin 9) and clocks both the ADC clock control flip flop (U21B in Block F) and the SRQ latch (U21A). The D input to the ADC clock control flip-flop (U21B) is grounded so it is reset which turns the clock off.

The D input to the SRQ flip-flop goes to HSRQ DISABLE (U29 pin 10). If HSRQ DISABLE is LOW then the SRQ flip-flop will be reset. The output of latch U21A goes to U22 in Block E to be read by the instrument processor and to a SRQ delay circuit which will allow only one ADC SRQ every 100 mS to limit the amount of main processor time devoted to servicing the ADC. LADC SRQ also goes to U6B pin 10 which disables the ADC clock until the SRQ is cleared by the RLEVEL strobe.

In the delay circuit, Q2 will be conducting any time the ADC is

not requesting service. As soon as ADC SRQ goes low, Q2 will be turned off and C53 will be charged up thru R42. When U19A pin 2 reaches its Vih, the output of U19A pin 3 will go low which signals the processor that a change has occured. As soon as the processor reads the ADC, the SRQ flip-flop will be set so its output (U21A pin 5) will go HIGH, Q2 will turn on and pull the input to U19A low and therefore its output will go back HIGH. R40 provides base drive current for Q2 since the output current of U21 would not be sufficient. R39 limits the discharge current of C53 when Q2 turns on.

The Change Detectors U19B and U19D are designed to output a low going pulse onto the LCHNG line to the digital interface board to indicate that a change has occured on the Unleveled or Overmod inputs to the Level Control board.

The inputs (LUNLVL and LOMD) also go to an output buffer (U22 pins 4 & 12 Block E) which can be read by the processor to determine what signal has changed state.

Let us assume that LUNLVL is HIGH initially; therefore both inputs to the LS266 open collector exclusive nor gate U19B will be HIGH. An exclusive nor gates output will go LOW when ever one and only one of its inputs are HIGH, therefore for the above conditions its output will be HIGH. When LUNLVL goes LOW, one input (U19B pin 6) immediately goes LOW while the other (U19B pin 6) remains above the trigger threshold due to the limited discharge rate of C41 thru R54. The output (U19B pin 4) will be low during this time. After some period of time, both inputs will be LOW. When LUNLVL goes HIGH, one input (U19B pin 6) will immediately go HIGH, while the other input (U19B pin 5) will remain below the trigger threshold for some period of time due to the charge rate of C41 thru R53 & 54. The output of the gate (U19B pin 4) will be LOW until the trigger threshold is reached.

The value of R54 and R52 were chosen so when LUNLVL or LOMD are LOW both inputs to U19 will be below the trigger threshold with worst case input currents to the gate. R53 and R51 then have been chosen to guarantee that the voltage divider formed with R52 and R53 will be above trigger threshold under worst case conditions.

ADC Control Latch Status Buffer X

There are several bits of information about functions on the Level Control board that must be communicated back to the instrument processor and several ADC control lines that must be asserted by the instrument processor.

A 74LS367 bus buffer (U22 Block X) is used to put several bits of information onto the data bus when the RSTAT strobe is pulled LOW

(U20 pin 7 in Block H). Four signals are communicated to the processor. They are LADCSRQ (U22 pin 14), LUNLVL (U22 pin 4), LOMD (U22 pin 12) and LOW BD INSTALLED (U22 pin 2).

A 74LS174 (U29 Block E) is used to latch six control signals off the data bus when the WADCC strobe (U29 pin 9) goes LOW. These signals are LOW CNVRT ALWAYS (U29 pin 2), LOW DON'T CNVRT (U29 pin 15), AMUX0-2 (U29 pins 5, 12 & 7) and HIGH ADC SRQ DISABLE (U29 pin 10).

ADC Clock/Control F

The clock for the ADC is generated by a schmidt trigger input NAND gate with RC feedback. The clock frequency is not critical and can vary by as much as 2:1 without causing any problems. This clock is controlled by several digital signals (U6B pins 10,12 & 13). Lets assume to start with that one of the clock control signals is LOW thus disabling the clock and the output (U6B pin 8) will be HIGH. When the output of this circuit is HIGH, the feedback input (U6B pin 9) will also be HIGH after a period of time. Now if the clock circuit is enabled, by all of the clock control signals going HIGH, the clock output (U6B pin 8) will immediately go LOW. The feedback input (U6B pin 9) will begin to head towards 0 volts at a rate determined by the RC time constant formed by R21 and C32. As soon as this voltage reaches the trigger threshold of the NAND gate, the clock output will go HIGH. The feedback input will head towards Vout at a rate determined by the RC time constant. As soon as this voltage reaches the trigger threshold of the NAND gate the clock output will again go LOW and the cycle will be repeated until one of the control lines (U6B pins 10,12 or 13) is pulled LOW.

Clock Control #1 (U6B pin 10) is connected to LADC SRQ so that the clock circuit is disabled whenever the ADC is being read. When the conversion is complete, the rising edge of the ADC clock (U6B pin 8) clocks the up/down counter (U1 pin 2 Block D) which causes its RCO signal (U1 pin 15) to go HIGH which in turn clocks the conversion complete flip/flop (U21A pin 3) causing ADC SRQ (U21A pin 5) to go LOW. The ADC clock must be disabled before the next falling edge of the clock to guarantee that there will be no partial clock pulses. Clock control #2 (U6B pin 13) is driven by the latched control line LOW DON'T CONVERT (U29 pin 15). This signal allows the instrument processor to prevent the ADC clock from running when it is not being used. Clock control #3 (U6B pin 12) is driven by the output of a NAND gate (U26D pin 11) used as a dual negative input OR gate.

If either input goes low, the clock circuit will be enabled. The first input (U26D pin 13) goes to LOW CNVRT ALWAYS. Any time this line is low, the clock will be enabled to run. The other input

(U26D pin 12) is driven by a four input NAND gate (U6A pin 6). IF LOW CNVRT ALWAYS is HIGH then the clock will be disabled when either input to U6A is LOW. The first input (U6A pins 1&2) are connected to the output of the conversion latch (U21B pin 9). The clock will be stopped when the conversion complete latch is reset which occures at the end of a conversion cycle. The other input to this gate (U6A pins 4&5) is connected to HADCEN (XA27P1 pin 8) which goes to the ALC circuitry and is HIGH only when a valid voltage representing the detected output power is present on the DETLVL line (XA27P1 pin 29). HADCEN has a pullup resistor (R59) so the ADC will function normally if the ALC board is removed.

Fail Test LED G

The Fail Test LED is used to indicate that an error condition has been detected on the level control board during self test using the ADC to check the major functional blocks on the board. This LED is turned ON and OFF by the processor.

Address Decoding H

The I/O strobe decoding consists of two 74LS138 3 line to eight line decoders (U20 & U27) and one NAND gate (U26A) connected as an inverter. These two decoders decode address lines A0 thru A4 and SIOA I/O strobe to produce input and output strobes for the RF section of the instrument.

20 GHz Breakpoint Slope Compensation I

The 20 GHz breakpoint is used to compensate for directional coupler forward losses and coupler detector coupling losses which occur at 20 to 23 GHz.

The breakpoint circuit is exactly the same as the 9 GHz breakpoint except the breakpoint will occur when the voltage on the V/GHz line is -10.0(R6/R7+R8).

The output of this breakpoint circuit is connected to the V referance input of a NE5018 DAC (U10 pin 14). This DAC is exactly as described for the attenuator slope compensation DAC or 9 GHz Breakpoint DAC.

Compensation Summing Amplifier J

The summing amplifier (U5A) sums four compensation terms together with the correct polarity and gain.

The Attenuator Slope Compensation is summed into the inverting input (U5A pin 2). This signal has a gain of [-(R13+R65)/R11=-2.5. The NE5018 DAC's have a voltage gain of 2

so the overall gain from input (R58 in Block N) to output (U5A pin 1) is -2.5(R1/R58)(2)=-4.13. One GHz Change in frequency will produce -.25 volts change of the V/GHz line and -4.13(-.25)=1.033 volts change at the output (U5A pin 1). The sensitivity of the LVLCOR output (U5A pin 1) is 1.25 dB/V so the above 1.033 volts represents a change in power of 1.033 V(1.25 dB/V)=1.29 dB. The above was assuming that the DAC was set at full range (input = 255). If we now want to know the affect that one bit change of the DAC has on the output we divide by the number of bits (256). The resulting sensitivity of the Attenuator Compensation DAC is (1.29 dB/GHz)/256 bits=.00504 dB/GHz/Bit which is approximately .005 dB/GHz/Bit.

The 9 GHz Slope Compensation is summed into the inverting input (U5A pin 2) with a gain of [-(R13+R65)/R10]=-1.0. The overall gain is [-2(R5/R2)(-1.0)]=2.0. One GHz change in frequency will produce .50 V change at the output. The resulting sensitivity of the 9 GHz Slope Compensation is [.50 V/GHz(1.25 dB/V)]/256 Bits=.0025 dB/GHz/Bit.

The 20 GHz Slope Compensation is summed into the inverting input (U5A pin 2) with a gain of [-(R13+R65)/R12]= -2.0. The overall gain is [-2(R9/R6)(-2.0)]=8.0. One GHz change in frequency will produce 2.0 V change at the output. The resulting sensitivity of the 20 GHz Slope Compensation is [2.0 V/GHz(1.25 dB/V)]/256 Bits=.01 dB/GHz/Bit.

Cable losses after the ALC detector must be accounted for by increasing the compensation voltage as a function of frequency. This cable loss increases with increasing temperature; therefore a temperature dependent frequency compensation must be summed in.

The Cable Loss TC Compensation is accomplished by summing a modified form of the V/GHZ voltage into the summing amp (U5A pin 2). R70 and R71 form a voltage divider which decreases the temperture compensation for front panel output options where the cable length is short. The amount of compensation at 25 degrees C is approx. .0027 dB/GHz. In the rear panel options where the cable length is long, R71 is removed and R70 is shorted to provide .0052 dB/GHz compensation at 25 degrees C. Since RT1's resistance decreases as its temperture increases, the amount of compensation increases with temperature.

ALC Reference Generator K

A 7520 type CMOS 10 bit multiplying DAC (U14) is used to control the reference voltage for the Level Control circuits.

The temperature accuracy of the entire leveling system cannot be any better than the reference voltage it receives therefore an

AD581L 10.00 v precision reference (Q1 in Block Q) is used for the reference into the level DAC. The T.C. of this device is less than 5 ppm. The +20 volt supply is used as the input voltage (Q1 pin 1) to minimize the load on the +15 V supply that is created on this board.

From this 10.00 volt reference, the level DAC (U14 pin 15) creates a current that is a function of the 10 bit digital input. Each LSB represents 1/1024th of the reference current. The current created above is a differential current between Iout1 (U14 pin 1) and Iout2 (U14 pin 2). Internal to the 7520 DAC (U14) there is a feedback resistor connected between Iout1 and R feedback (U14 pin 16). This resistor's value tracks the T.C. of the current produced by the DAC.

Iout1 is connected to the inverting input of the output op-amp (U17 pin 2). Iout2 is connected to the non-inverting input of this op-amp (U17 pin 3) and to reference ground. The feedback resistor (U14 pin 6) is connected to the output of the op-amp (U17 pin 6).

If we consider the op-amp ideal, then the voltage at Iout1 must be zero; furthermore, the input current to the op-amp must be zero. The current sourced by the DAC must go somewhere and therefore the op-amp produces a voltage at its output that is exactly sufficient to sink this Iout1 current through the feedback resistor. This produces a voltage drop that is proportional to Rfeedback. A larger digital value increases Iout1 in proportion, and the voltage at the output of the op-amp (U17 pin 6) must become more negative to sink the appropriate amount of current thru Rfeedback.

From the above we can conclude that the voltage produced at the output will be negative and will be between 0 volts and (1023/1024)Vref.

A schottky diode (CR8) is placed accross the Iout1 and Iout2 pins of the DAC. This prevents the voltage at these pins from exceeding the supply voltage during turn-on which would cause latch-up.

The digital inputs to this DAC are latched off of the instrument data buss by two 74LS174 6-bit latches (U13 & U16). The clock for these latches is the WLEVEL strobe (U27 pin 14 in Block H). The outputs of these latches are pulled up to the 5 volt supply with 1K ohm resistors. These pullups reduce the magnitude of digital noise feeding through the latches by pulling each output up hard to the supply.

Reference-Level Summing Amplifier

The output from the Level DAC and the Level Sweep DAC are summed together at unity gain by the summing op-amp (U18B). The +10.00 reference is also summed into this op-amp with a gain of .5 to provide a negative 5 volts offset at the level reference output (U18B pin 7). The output can be adjusted between approximately -5.12 and +5.11 volts by the main Level DAC. This voltage represents a change in output power of +25.55 dBm to -25.60 dBm and represents a slope of approximately -.2 volts/dB. This is approximately because the exact slope and offset of the level reference is corrected in software by the instrument controller.

9 GHz Breakpoint Slope Compensation M

At about 9 GHz the detector's specifications indicate that it could have either increasing or decreasing output versus frequency. Since the detector's specifications indicates that either situation could occur from unit to unit, a bipolar breakpoint was placed at approximately 9 GHz.

When we talk about creating a correction to the level reference voltage to compensate for detector losses, we must remember the following. If the output of the detector decreases for any reason, the ALC circuitry will INCREASE the output power to force the detector output to be the same. So to compensate for dector losses we must create a correction that decreases the level reference.

The location of the breakpoint (the frequency at which the correction begins to occur) is controlled by an amplfier with diode feedback paths. An op-amp (U4B) has a diode (CR3) in series with its output (U4B pin 7) so whenever its output voltage is less than zero volts the diode will be reverse biased. Furthermore a diode clamp (CR2) clamps its output (pin 7) to no more negative than one diode drop. When its output (pin 7) is positive, the series diode (CR3) is forward biased, the diode clamp (CR2) is reverse biased and the op-amp is now in a standard inverting gain configuration with a 10K feedback resistor (R5). The V/GHz line (-.25 V/GHz) and an offset are summed into the inverting input of the op-amp (U4B pin 6). The offset resistor (R3 + R4) is connected to the +10.00 volt precision reference. The input resistor (R2) is connected to the V/GHz line. As long as the current provided by the offset resistor (R3 +R4) is greater than the current sunk by the input resistor (R2), the output of this circuit will remain at 0 volts. As soon as the current sunk by the input resistor is greater than that provided by the offset resistor, the output of the circuit will begin to increase at a rate of +.25 V/GHz since the amplifier has a gain of 1. The breakpoint will occur when the voltage on the V/GHz line equals 10.0 V(R2/R3+R4). The offset resistor is a fixed

resistor in series with a pot so the point at which the breakpoint occures can be adjusted over some range.

The output of this breakpoint circuit is connected to the V reference input of a NE5018 DAC (U9 pin 14). This DAC is exactly the same as the attenuator slope DAC. When the digital input is 0 the output is -V reference, when the digital input is 128 the output will be 0 volts and when the digital input is 255 the output will be +(127/128) V reference.

Attenuator Slope Compensation N

Attenuator slope compensation is used to increase or decrease the level reference voltage as a function of frequency. When this reference is increasing, it causes the leveling circuitry to increase the output power as a function of frequency to compensate for power losses in the attenuator or cabling between the detector coupler and the output of the 8340A.

In LOW Band this reference is decreasing. This causes the leveling circuitry to decrease the output power to compensate for the frequency response of the LOW Band detector.

The rate at which the output power increases is determined by the number written into the attenuator slope compensation DAC (U8). This number may be different for each RF attenuator step if their frequency characteristics are different.

The frequency reference for this circuit is the V/GHz line which comes from the A28 SYTM driver board. The voltage on the V/GHz line is -.25 volts per GHz and is derived from the pretune voltage and is modified by the band number.

This V/GHz line goes into an inverting amplifier (U5B pin 6) which has a gain of -(10/12.1). This gain block is necessary since the reference voltage required at the DAC (U8 pin 14) must be positive.

The Signetics NE5018 DAC is used for all three compensation DACs (U8, U9, and U10). It contains input latches and an output buffer. Inside this DAC, the reference voltage is converted into a reference current for the R-2R DAC ladder network.

Digital data is latched off of the data buss when the Latch Enable signal (U8 pin 10) goes low. This latched data controls the current switches inside the DAC to produce a current that is proportional to the Reference voltage and the latched digital information. This current is then fed into a current to voltage conversion stage and appears at the output (U8 pin 18) as a voltage which is proportional to the voltage on the V/GHz line

and the digital information.

The diode (CR1) connected to the summing node of the DAC (U8 pin 20) prevents the summing node from droping more than a diode drop below ground and therefore improves the DACs settling time.

A capacitor (C10) is connected in parallel with the internal feedback resistor (U8 pins 18 and 20) provides high frequency stabilization under all conditions. Another capacitor (C9) is connected between the summing node and the amplifier compensation pins (U8 pins 20 and 21) and is required to make the output amplifier as fast as possible while still remaining stable.

Power Sweep Generator Q

The level sweep DAC provides the power sweep function by sweeping the level reference as a function of the sweep ramp. This feature may also be used by the customer to compensate for line length external to the 8340A.

The level sweep DAC (U24) is implemented exactly the same as the level DAC (U14) except that its reference voltage (U24 pin 15) is the RF Sweep ramp that linearly varies between 0 and +10 volts as the frequency sweeps between the start and stop frequency. This input is clamped to ground and VDD by two schottky diodes to prevent any latch up problems. The output op-amp (U31) and the input latches (U23 & U30) are implemented exactly the same as the main level control DAC.

Band Switch Control P

A 74LS175 latch (U28) is used to latch data bits 0,1 & 2 off of the data buss when WBAND strobe (U27 pin 13 Block H) goes LOW and then HIGH. These latched data bits produce the encoded latched band information HLB0 (U28 pin 2), HLB1 (U28 pin 7) and B2 (U28 pin 10).

LHET is decoded by using a NAND gate as a dual negative input OR gate (U26B). The inverting outputs of latch (U28) HLB1-not (U28 pin 6) and HLB2-not (U28 pin 11) go to this OR gate and cause its output (LHET U26 pin 6) to go HIGH when either input (U26 pin 4 or 5) goes LOW.

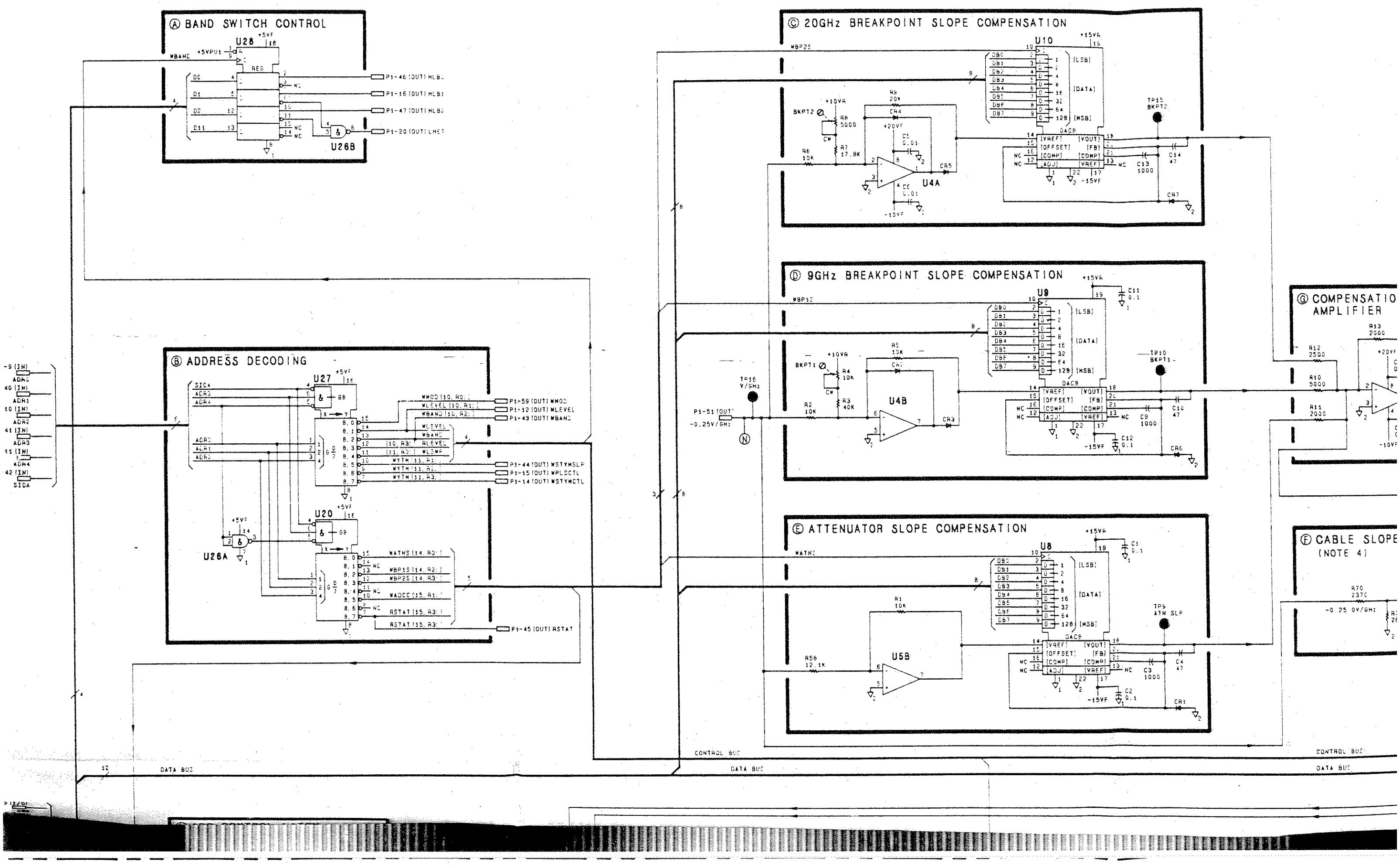
Power Supplies Q

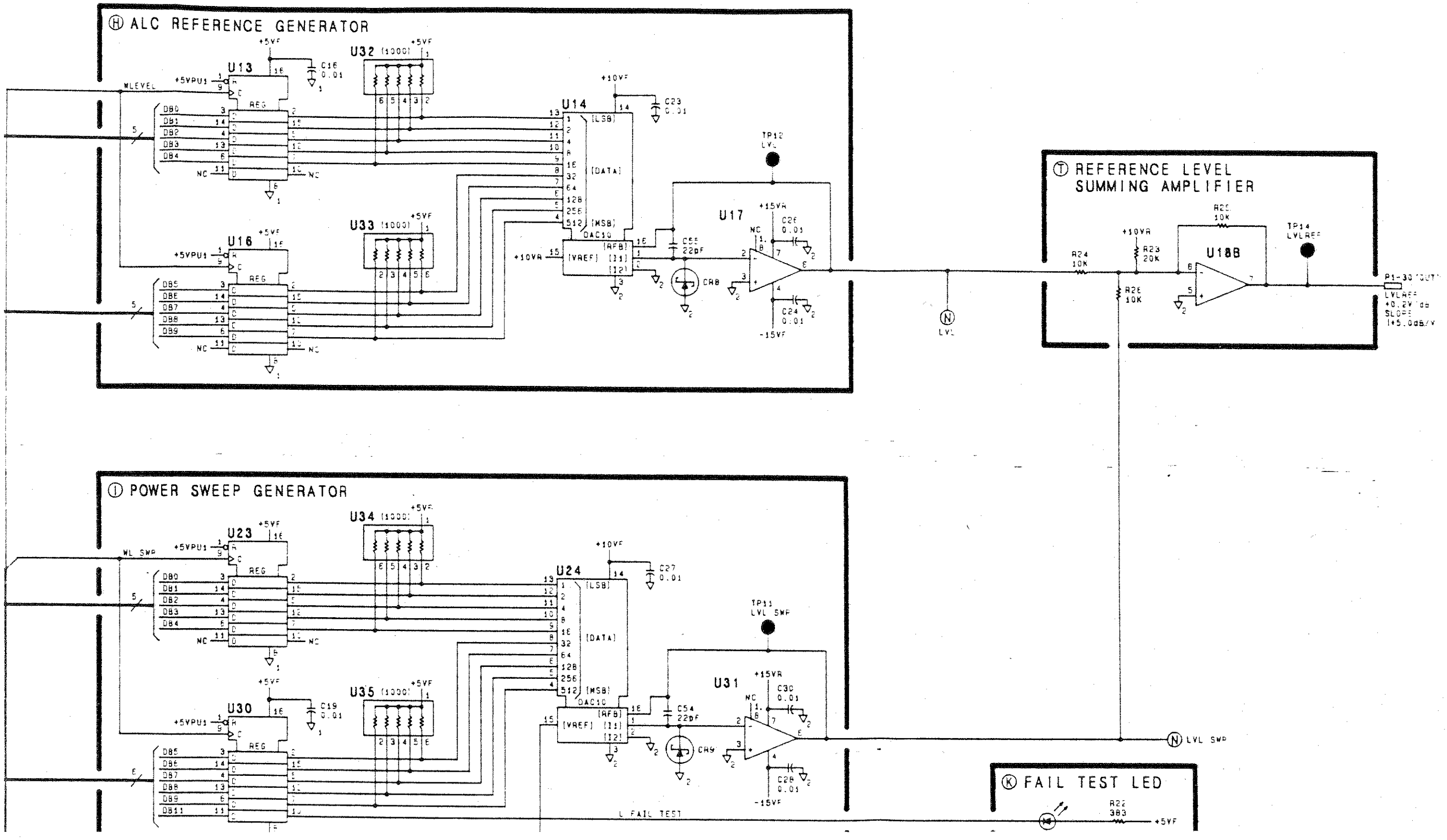
There is nothing unusual about the power supply filtering for the +20V, +5V, -5V, -10V or -15V supplies. Standard Low Q filters were used to help prevent resonances. A +15 V supply is provided using a 3 terminal adjustable regulator (Q3). In addition to all of the above supplies, a low current +10V supply to be used by

the CMOS 7520 DACs U8, U9, and U10. The reliability of these CMOS DACs should increase as the voltage stress is decreased as far as practical. This 10V supply is tied to the +5.2 V supply to prevent the digital inputs to the DACs from being greater than the VDD supply during turn-on.

R57 is used to remove D.C. currents from the Reference Ground. These currents are injected by the DACs and other resistors connected to this ground.

FLATNESS COMPENSATION




Ⓗ ALC REFERENCE GENERATOR
WLEVEL
U13
U16
U32 (1000)
U33 (1000)
U14
U17
REG
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
DB8
DB9
NC
+5VF
+5VPU1
+10VF
+10VR
+15VR
-15VF
C16 0.01
C23 0.01
C55 22pF
C26 0.01
C24 0.01
CR8
TP12 LVL
[LSB]
[DATA]
[MSB]
DAC10
[RFB]
[VREF]
[I1]
[I2]
Ⓣ REFERENCE LEVEL SUMMING AMPLIFIER
R25 10K
R24 10K
R23 20K
R26 10K
U18B
TP14 LVLREF
P1-30 (OUT) LVLREF +0.2V/dB SLOPE 1+5.0dB/V
Ⓝ LVL
Ⓘ POWER SWEEP GENERATOR
WL SWP
U23
U30
U34 (1000)
U35 (1000)
U24
U31
C27 0.01
C19 0.01
C54 22pF
C30 0.01
C28 0.01
CR9
TP11 LVL SWP
DB10
DB11
Ⓝ LVL SWP
L FAIL TEST
Ⓚ FAIL TEST LED
R22 383

Ⓛ ADC CONTROL LATCH

U29 — +5VF — C21 0.01 — MADCC — +5VPU1

REG

DB0	3	2	L CONVERT ALWAYS
DB1	14	15	L DON'T CONVERT
DB2	4	1	LA MUX0
DB3	13	12	LA MUX1
DB4	6	7	LA MUX2
DB5	11	10	M SRQ DISABLE

12 — 6 — 3

DB0 (I/O) … DB11 (I/O)

Ⓜ ADC CLOCK/CONTROL

L A-D SRQ
L DON'T CONVERT
L CONVERT ALWAYS

P1-8 (IN) HADCEN — TP2 HADCEN — +5VF — R59 10K — R67 10K

U6A — U26B — U6B — TP3 CLK — A-D CLK

R21 825 — C32 0.0015

U21B — NC — FF

U19C — L OUTSIDE WINDOW

Ⓢ POWER SUPPLIES

P1-2, 33 (IN) +20V — L1 10C — C43 4.7 — +20VF

HEAT SINK — Q3 VOLT REG (IN, OUT, GND) — TP8 +15 — +15VR — C44 1.0

Q1 VOLT REF — +10V — +10VR

R55 1000 — CR13 — +10VF

VR1 11.0V — CR12

P1-3, 34 (IN) +5.2V — L4 10 — C49 10 — C50 0.1 — +5VF

R66 1000 — +5VPU1

R68 511Ω — +5VPU2

P1-6, 37 GND — R56 10 — P1-18, 28, 48, 60 RGND — TP6 REF GND

TP1 DIG GND — P1-7, 19, 38, 50 GND

P1-1, 32 (IN) -5.2V — L3 10C — C47 6.8 — C48 0.1 — -5VF

P1-4, 35 (IN) -10V — L5 10C — C51 6.8 — C52 0.1 — -10VF

P1-5, 36 (IN) -15V — L2 10C — C45 4.7 — C46 0.1 — R57 316Ω — -15VF

Ⓝ ADC INPUT MULTIPLEXER

U25 — +20VF — LA MUX0 — LA MUX1 — LA MUX2 — +5VF — A 0/7 — MUX

TP20 DETLVL -.2V/dB 0V=0dBm — R28 50K — P1-29 (IN) DETLVL

LVL COR (G) — R29 50K

LVL (H) — R30 50K — R63 100K — +10VR

LVL SWP (I) — R31 50K — R64 100K

-0.25V/GHz (D) — R32 12.5K — R61 100K

TP21 BVSWP — R33 50K — R62 100K — P1-31 (IN) BVSWP

TP19 MODLVL — R34 35K — R59 562K — P1-61 (IN) MODLVL

TP17 A-D INB — R36 50K — R35 50K — -10VF

TP7 A-D IN — R38 50K — +20VF — C33 0.01 — U18A — C34 0.01 — -10VF

Ⓞ TEST ADC

+5VF — U12 — EN1 — EN2 — BUF

U11 — [CLOCK] — [DATA HOLD] — [DATA SHIFT] — [OUTPUT ENABLE] — ADC10

[IREF] — [+REF AMP] — [-REF AMP] — [REF AMP COMP] — [DATA] — [IOUT] — [COMP IN] — [COMP REF] — [VREF GND] — [VREF]

+10VR — R17 10K — R16 10K — R18 5000 — C31 1.0 — R43 2500 — R19 1000 — R20 619 — R15 10K

DIFFERENCE — P1-39 (IN) LATTN

U15 — EN1 — EN2 — BUF

Ⓟ ADC WINDOW COMPARATOR

+10VR — R47 10K — R48 75 — C39 0.1 — (+75mV) — U2 — COMP — +20VF — -10VF — +5VF — R5 10

U7 — DIFFERENCE — C35 0.01 — C37 0.01 — R44 100K — R45 5110

R49 100Ω — C38 0.1

R50 75 — (-75mV) — U3 — COMP — R46 10K — C40 0.1

A-D CONVERTER

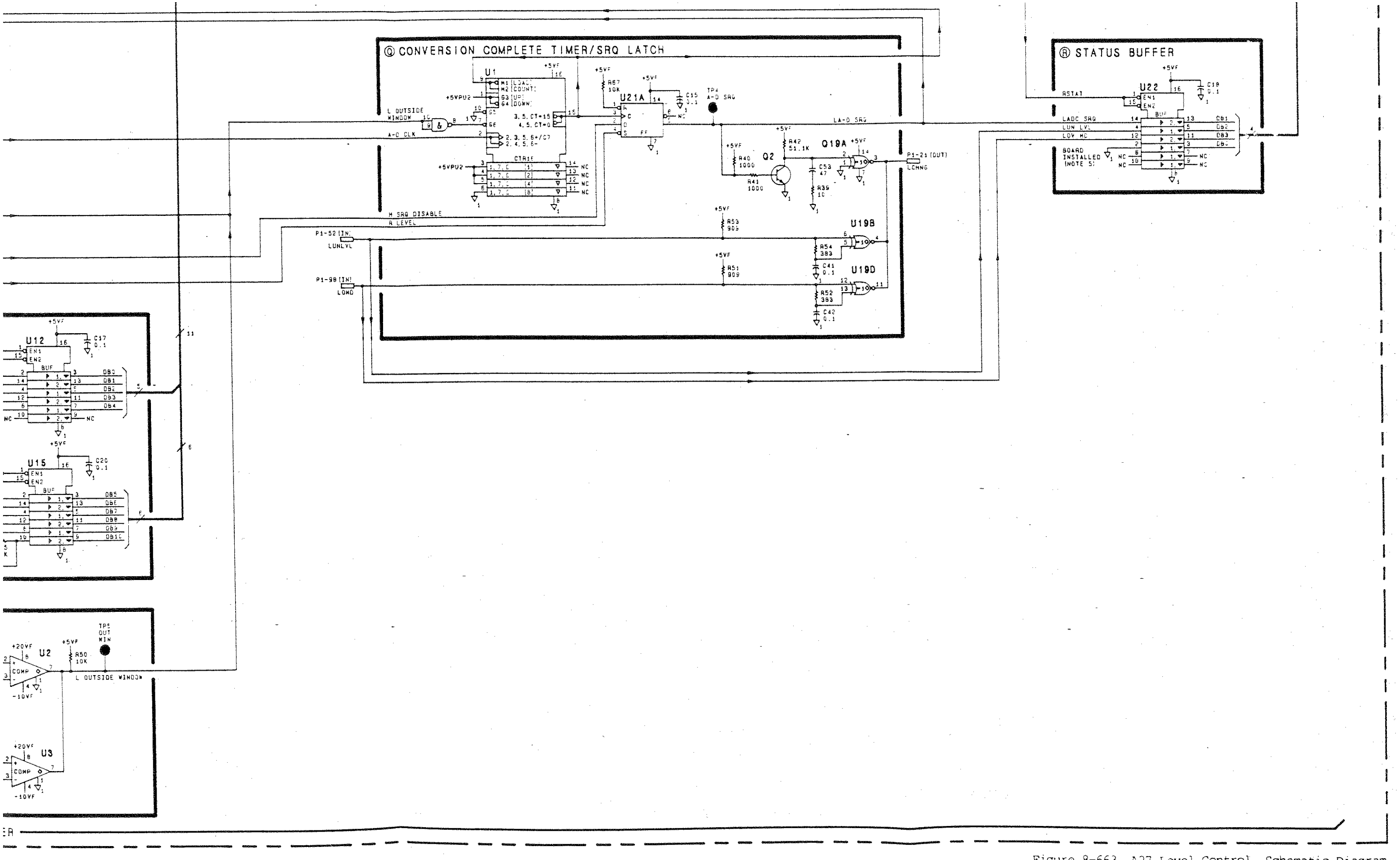


Figure 8-663. A27 Level Control, Schematic Diagram

A28 SYTM DRIVER, CIRCUIT DESCRIPTION

Introduction

The SYTM Driver provides the correct amount of current to the SYTM coil to track the YO frequency under all conditions. Since the SYTM uses an open-loop tracking scheme, all differences in tracking conditions must be compensated for by the SYTM driver without the benefit of feedback. The SYTM driver also provides the rest of the instrument with voltages that are proportional to frequency (-0.25 V/GHz, +1.0/+0.5 V/GHz, +1.4 v/GHz).

Offset Compensation A

The offset compensation circuitry adds a correction current independant of frequency. The offset, adjusted by R1, affects the entire operating range of the SYTM and has a range of ±200 MHz. A separate offset adjusted by R113 is active only in band 1 (switched by Q4) and has a range of ±150 MHz that is superimposed on the setting of R1.

Delay Compensation B

The SYTM magnet responds to any change in coil current, by setting up eddy currents to oppose the change. During a sweep, while the input current is ramping, the eddy currents set up a magnetic field that partially cancels the magnetic field required to tune the SYTM passband. A compensation current proportional to (A+BFs)dF/dt (where Fs is a term that represents the frequency change from the start of sweep, dF/dt corresponds to the sweep rate, and where A and B are constants) is added to the current driving the SYTM in order to offset the effects of the eddy currents. Since the eddy currents take time to set up, the start of the compensation ramp needs to be rounded. Although the transient response of the eddy currents doesn't appear to follow an exponential function, using a low-pass filter on the delay compensation adaquately accounts for the transient response.

The delay DAC (U3) gives the instrument processor control over the gain of the delay correction. When the processor writes to IO address 10,R2: a strobe (WBAND) is generated on the A27 Level Control Board. WBAND comes onto the SYTM driver through P1 Pin 29. When WBAND is pulsed, U14 latches the information on bits 3 through 10 of the Data Bus. The latched bits form the binary input to the delay DAC (U3). The reference input to the delay DAC is the sum of inputs coresponding to the A and BFs terms discussed in the first paragraph of this section. When Q10 is closed the voltage across C13 is self-adjusting to give 0V output from U5A. When Q10 is opened, the output of U5A is proportional to the -0.25 V/GHz line, offset by the voltage across C13. When

the instrument is sweeping, this generates a ramp that is referenced to the frequency at the time Q10 was opened. Q10 is open when HSP (P1 Pin 26) is high. The output voltage at U5A is summed into U2A through R7 (DYS) to give the BFs term for the delay compensation. The offset term A is adjusted through R6 (DYO) and summed into U2A as well. If the 8340A is sweeping 19.8 GHz to 26.5 GHz and if R6 (DYO) and R7 (DYS) are both turned fully counter-clockwise, then the output of U2A pin 1 will ramp up to about +9.7 V. R55 converts the output of U2A into the reference current (Iref) for the delay DAC (U3). Iref causes an equal current to flow from a series of binary weighted switches in U3. The binary switches are driven by the latched bits from U14. The internal binary weighted switches source the current from U3 pin 4 when the latched bits corresponding to the switches are HIGH.

When the latched bits are LOW the current is sourced from U3 pin 2. Thus when all of the latched bits are HIGH, U3 pin 4 will sink a current equal to Iref and U3 pin 2 will not sink any current. When all of the bits are LOW U4 pin 2 will sink a current equal to Iref and U3 pin 4 will not sink any current. The amount of current sunk by U3 pin 4 (I1) and U3 pin 2 (I2) will vary between the two extremes in proportion to the latched binary code with the sum of I1 and I2 equal to Iref. The voltage present at U2C pin 8 is equal to I1^*2K. In terms of the input current this becomes Iref^*N^*2K where N is the ratio of the binary input to the full scale binary input to the DAC. This gives (A+BFs)dF/dt to compensate for the eddy current delay. Q9 switches the delay compensation into the compensation summing amplifier at appropriate times. Q9 is on when HSP (P1 pin 26) is HIGH. Since HSP is also HIGH in CW the delay DAC (U3) is programmed to 0 by the processor because no delay compensation is required in CW operation. R46, R47 and C26 form a low-pass filter that rounds the first part of the delay compensation waveform.

Slope Compensation C

The slope compensation circuits generate a correction current proportional to frequency. The slope DAC (U4) provides microprocessor control over the slope correction and enables the 8340A to do the required self-peaking (see Block H description). When the processor writes to I/O address 11,R1: a strobe (WYTMSLP) is generated on the A27 Level Control Board. WYTMSLP comes onto the SYTM driver through P1 pin 30 and causes U15 to latch the binary input for U4. The reference input for U4 is the PRETUNE signal that has been scaled and inverted by U2B to give +1.4 V/GHz ±1%. This voltage is also output from P1 pin 7 and is used for the ramp bias of the step recovery diode in the SYTM.

The voltage present at U2D pin 14 is equal to the combined

effects of I1 (current sunk by U4 pin 4) and I2 (current sunk by U4 pin 2). The two current effects can be considered independantly and then added for the final result. To consider the effects separately, set one equal to zero and look at the effects of the other. No current will flow through R57 due to I1 so the voltage at U2D pin 14 due to I1 will be equal to -2K^I1. No current will flow through R58 due to I2 so the voltage at pin 14 due to I2 will be 2K^*I2. The voltage at U2D pin 14 due to both currents will be 2K^*(I2-I1). I1+I2=Iref and I1=N^*Iref (where N is the ratio of the binary input to the full scale binary input to the DAC). This gives a final result for the output voltage of U2D pin 14 to be PRETUNE^*4/8.9±1.3%)^*(1-2^*N). The output voltage of U2D pin 14 can vary by as much as ±7.97V which is summed into the compensation amplifier in Block G through R56. The output voltage on pins 2 and 4 of U4 can vary between -7.97V and 0V which is within the output voltage compliance of U4 (-8.1V and +21V). The DAC provides ±4% slope adjustment in band 1, ±2% in band 2, ±1.3% in band 3 and ±1% in band 4.

Since bits 0 through 2 are ignored when the data is latched into U15 from the data bus the binary pattern present at the input of the delay DAC increments once for every eight increments of the data on the Data Bus. Whenever the RPG is connected to U4 it will take eight pulses of the RPG to change the DAC by one bit. This will give a less sensitive feel to the RPG.

In addition to the correction provided by the slope DAC, three breakpoints are provided to correct for the non-linearities of the SYTM magnet B-H curve. R20, R21, R22, R18 and R17 form a voltage divider used in conjunction with CR1 and CR2 to set fixed frequency breakpoints at 13.7 GHz (±2%) and 20 GHz (±2%). R2 and R3 vary the effect of the breakpoints adding as much as 3.1% and 3.2% respectively. R4, R5 and CR3 form a breakpoint that can be varied in frequency (anywhere above 23.2 GHz) as well as adjusted to add as much as 4.0% to the slope. All percentage increases in slope are referenced to the frequency where the breakpoint begins to take effect.

Programmable Scaler D

The Pretune line comes to the SYTM driver board on P1 Pin 22. It is a voltage proportional to YO frequency and is adjusted to give -2.5 v/GHz with an accuracy of ±6.5mV ±7uV/degrees C -25ppm/degrees C.

The programmable scaler uses a precision resistor array (U21) to attenuate the PRETUNE voltage giving a voltage that is proportional to SYTM frequency. The overall accuracy depends on the accuracy of the PRETUNE line as well as that of the resistor

array. Hence, the specifications for the resistor array are important to the accuracy of the -0.25 V/GHz and +1.0/+0.5 V/GHz lines as well as to the tuning of the SYTM. The array consists of eight 2.5K resistors with a 5% absolute tolerance, .01% tracking tolerance relative to R1 (giving a worst case tolerance of .02% for any resistor ratio). The array also has a 2ppm/degrees C tracking temperature coefficient between any two resistors.

The latched band information (P1 Pins 31, 32, and 33 in Block I) is used as the input for a 3 by 8 decoder (U16). The outputs of the decoder are input into comparators (U19) that drive the gates of FETs to switch the appropriate node of the scaler. Band 1 is the node activated during the fundamental band of the 8340A. When this node is selected the impedance looking into the scaler is 1.6K. The output voltage is given by:

$$Vout=PRETUNE(1\pm0.047\%\pm4.7ppm/degrees\ C)/10$$

Over a 45 degrees C temperature rise at 7 GHz, the worst case error is 3.9mV which represents an error of $\pm$16 MHz.

Band 2 is the node activated during the 2nd harmonic band of the 8340A. When this node is selected the impedance looking into the scaler is 1.3K. The output voltage is given by:

$$Vout=2\hat{}*PRETUNE(1\pm0.032\%\pm3.2ppm/degrees\ C)/10$$

Over a 45 degrees C temperature rise at 13.5 GHz, the worst case error is 6.7mV which represents an error of $\pm$27 MHz.

Band 3 is the node activated during the 3rd harmonic band of the 8340A. When this node is selected the impedance looking into the scaler is 2.6K. The output voltage is given by:

$$Vout=3\hat{}*PRETUNE(1\pm0.03\%\pm3ppm/degrees\ C)/10$$

Over a 45 C temperature rise at 20 GHz, the worst case error is 9.8mV which represents an error of $\pm$40 MHz.

Band 4 is the node activated during the 4th harmonic band of the 8340A. When this node is selected the impedance looking into the scaler is 2K. The output voltage is given by:

$$Vout=4\hat{}*PRETUNE(1\pm0.024\%\pm2.4ppm/degrees\ C)/10$$

Over a 45 degrees C temperature rise at 26.5 GHz, the worst case error is 12.5mV which represents an error of $\pm$50 MHz.

-0.25 V/GHz E

The -0.25 V/GHz line is the most widely used signal on the SYTM driver board. During HIBAND (Bands 1-4) it is a buffered version of the voltage out of the programmable scaler. U6 has a low offset voltage (1.6mV max over 0 C-70 C) and keeps the output within 1.6mV (6.4 MHz) of the input signal. During LOBAND ,Band 0, (Q11 closed and Q18 open) the instrument frequency is equal to the YO frequency offset by 3.7 GHz. The -0.25 V/GHz line uses the PRETUNE voltage, scales it down to -0.25 v/GHz and adds an offset voltage that equals .25 v/GHz^*3.7 GHz or .925V. This signal is generated using the +10V reference, offset R68, R69, and R70, and PRETUNE. When the LOBAND signal is adjusted at 10 MHz by trimming the +10V reference with R85 (Block K) the -0.25 V/GHz line will be accurate within 7 MHz of the ideal value at 2.2 GHz (including the resolution of the 12 bit PRETUNE DAC).

The worst-case error of 30 MHz occurs at 2.3 GHz over a 45 degrees C temperature change.

Q11 and Q18 switch between the LOBAND and HIBAND conditions. A sample and hold circuit (Q5 and U5B) is used to remove the discontinuities that are present due to changing the band number and PRETUNE at different times.

Q6 is capable of sourcing 2mA and sinking 40mA. The normal load requires sinking 7mA and sourcing 0.32mA. R65 limits the amount of output current to protect Q6 in the event the output is shorted. R27 along with the +20V supply provide the sourcing capability. C16 is required to stabalize the loop during the sample mode. The holding capacitor (C14) is a mylar capacitor with an insulation resistance of 15,000 megohms. U5B has a maximum input bias current of 8nA over 0 degrees C to 70 degrees C (100 pA at 25 degrees C). Q5 has a maximum drain cutoff current of 0.1nA. The maximum droop is 260 mV/sec. A normal holding interval is about 5 msec resulting in a maximum droop of 1.3mV during the holding interval. This value drops substancially at instrument temperatures lower than 70 degrees C. The maximum droop at room temperature is 20 mV/sec or 0.1mV during a holding interval of 5 msec. When the circuit is in the hold mode (Q5 open) R32 and diodes CR4 and CR5 keep U6 from saturation and making the output of U6 a buffered version of the input to U6. The output of U6 is used as a pullup voltage for the comparators driving the FET's in Blocks D (Programmable Scaler) and E (-0.25 V/GHz). The output of U6 also drives the guard trace described in the Current Driver description (Block H). Without the clamping provided in the hold mode, the input diode protection of U6 would shunt current along the input disturbing the desired SYTM tuning. Because U6 doesn't saturate, the transition from hold to sample occurs with a minimal perturbation. R33 attenuates the amplitude of the hold-to-sample perturbation. R30 eliminates the ringing of the perturbation.

+1.0/+0.5 V/GHz F

This block provides a voltage proportional to instrument frequency that is sent to the rear panel. The standard configuration has a sensitivity of +1.0 v/GHz. This limits at around +19V (+20V supply tolerance and 0.4V saturation across Q7). The +1.0 v/GHz sensitivity is necessary to interface with 8410 Series Network Analyzer. The limit of +19V doesn't matter in this case because the 8410 only covers up to 18.6 GHz. For applications involving the entire frequency range, 2 jumpers (W1 and W2) on the SYTM driver board can be removed to change the sensitivity to +0.5 v/GHz.

Q8 and R37 provide a current source that limits at approximately +19.7 volts. The current is on the order of 1.2mA (not exact because the transistor parameters of each half will differ due to the difference in their power dissipation). This current in conjunction with R41 will give about a +5 volt offset from the output of U10. This removes the effect of op amp limiting which happens as low as +17V for U10. C19 insures that the 0dB gain crossover for the loop has a slope of -6dB/octave. Q7 is a dual npn transistor, one side Q7B is used as a drive transistor for the output, the other side is used in conjunction with R38 to limit the output current to 7.8mA. CR6 and CR7 protect the circuitry from voltages that may inadvertantly be applied to the output. R73 and the -10V supply provide pulldown capabilities for the output. R75 with R40 and R39 cause the output to be referenced to the ground potential at the rear panel. R42, R43, C20 and C21 are used for high frequency noise rejection of the power supplies.

Compensation Summing Amplifier G

The currents that are generated by the slope, offset and delay compensation circuitry are amplified by a factor of 25 by U1 and injected into the collector of the drive transistor A47Q2. The effect of R13 is that of paralleling R13 across the sense resistors on the A47 assembly plus adding an additional current equal to the voltage at the emitter of Q1 divided by R13. Q1 is used to buffer the output of U1 to allow the amplifier to have a higher output voltage capability. R11 and the -10 volt supply provide a sink capability. The compensation summing amplifier U1 is able to pull the passband of the SYTM over the range of -220 MHz to +625 MHz. Q3 is a p-channel FET used to switch the compensation out during kick pulses (see Block J). Q2, R116 and R117 drive the gate of Q3 to +20 volts to turn it OFF and to 0 volts to turn it ON.

Current Driver H

When considering the errors of the current driver, only the temperature effects need be considered since the steady-state errors are adjusted out when the instrument is calibrated.

The temperature errors indicate the need for a self peaking routine for the 8340A. The 1dB passband is on the order of 25-30 MHz in band 4, assuming the instrument is calibrated to center the tracking in the middle of the passband, the errors that could result from a temperature drift would cause power losses greater than any tolerable level.

The sensitivity of the input node of the current driver is 4 MHz/mV. The impedance of the line can be as much as 2.6K. In order to keep the errors due to leakage currents less than 1 MHz, the leakage currents must be kept below 100nA, otherwise potential problems could exist. To avoid the problems, guard traces are placed around the sensitive traces. The guard traces are driven by a buffered version of the same voltage.

A triple darlington configuration (Q26, Q27, and drive transistor A47Q2) is used to remove the effects of the variation of the beta of the drive transistor due to temperature. With the triple darlington configuration, the base current into the OP-07 (U22) is less than 15uA so any variations in this current due to temperature would influence the tracking by less than 1MHz. R110 and R100 are used to keep a small amount of current flowing through Q26 and Q27.

Due to the inductance of the SYTM coil, a voltage spike is generated when the current ramp is reset. The zener diode, VR2 prevents this voltage kick from exceeding the breakdown voltage for the transistors by controlling the maximum allowed rate of change of current from the driver. CR10 protects the base-emitter junction of Q26 from large voltages that could cause a breakdown. CR11 is a low capacitance diode that is placed in series with VR2 to reduce the effect of the zener diode's junction capacitance. R111 is added to eliminate the ringing that would otherwise be present at retrace. There is also a zener diode protection circuit on the SYTM bias board. This circuit clamps the inductive voltage at a higher voltage (about 140V) than the one on the driver board (about 125V). The primary purpose for this cicuit is to protect the drive transistor located on the A47 Sense Resistor assembly in the event that someone removes the A28 SYTM Driver board while the instrument is under power.

The breakdown voltage of the drive transistor is 400V. Q26 and Q27 have breakdown voltages of 160V so the clamping circuit on the bias board would also protect them if the clamping circuit on the driver board fails. Due to the method employed by the

clamping circuit on the SYTM driver, the sense resistors always give an indication of the amount of current flowing through the coil. This voltage is used by the kick pulse comparators to sense the amount of current in the coil. If the clamping circuit on the driver board fails, there would be no negative (in frequency) kick pulse and the delay compensation wouldn't be as effective. However the rest of the circuit would work because the clamping circuit on the SYTM bias board would protect the transistors.

Since the sensitivity of the SYTM's can vary from 14.2 mA/GHz to 16 mA/GHz, the gain of the current driver must be able to accomodate that range. The SYTM driver can tune between 14 mA/GHz and 16.5 mA/GHz.

The output drive stage is limited in current drive capability due to the voltage rails. The critical factors are:

Maximum voltage across the sense resistors	798V
Maximum saturation voltage of transistors	2.25V
Additional drop due to wiring from 40V sense	0.22V
Minimum voltage across drive strip	39.45V
Inductance of coil	about 0.6H
Maximum sweep rate	600 MHz/msec
Resistance of coil at 25 degrees C	about 42 ohms
TC of coil resistance	+0.545%/degrees C
Current not sensed in sense resistors	about 12mA

C39, C40, and R101 are used to match the frequency response of the SYTM coil to the frequency response of the YO coil. The sweep output on the front and rear panels is also matched.

During a bandswitch the -0.25 V/GHz voltage is more accurate for holding the SYTM at the desired current than is the normal attenuated PRETUNE voltage (see Block H). At these times the -0.25 V/GHz line is gated by Q12 to override the attenuated PRETUNE voltage to hold the SYTM and avoid the undesired kick pulses that would be present due to the discontinuities on the attenuated PRETUNE line. When the instrument is in Band 0 the SYTM magnet is tuned to about 4GHz to keep the yig sphere from interferring with the output. Tuning the SYTM to 4GHz is accomplished by closing Q17. R109, Q21, and Q25 will be discussed under Kick Pulses (Block J).

Digital Control I

The following digital control signals are used on the SYTM driver board:

HSP: (P1 Pin 26) A signal from the A59 Digital Interface board

that is high when the instrument is sweeping and low at bandcrossings and retrace. HSP is used to generate the DELAY and DLY RES signals which control Q10 and Q9 in Block B.

WBAND: (P1 pin 29) (10,R2:) Block B - A strobe from the A27 Level Control board used by U14 to latch data from the Data Bus for U3 (delay DAC).

WYTMSLP: (P1 pin 30) (11,R1:) Block C - A strobe from the A27 Control board used by U15 to latch data from the data bus for U4 (slope DAC).

WYTMCTL: (P1 pin 8) (11,R3:) Block I - A strobe from the A27 Level Control board used by U13 to latch S/H from Data Bit 3, SYTMSEL from Data Bit 4, KICK TRIGGER from Data Bit 5.

KICK TRIGGER: (U13 pin 7 Block I) Initiates the SYTM kick pulse in Block J when set momentarily HIGH. KICK TRIGGER is a pulse that is about 20 usec wide.

SYTMSEL: (U17B pin 1) controls the gate signal for Q12 in Block H.

S/H (DB3), LYTMKICK, and LYOKICK (P1 pin 41): Used by U12A (Block I) to generate the sample signal which controls Q5 in Block E.

HLB0 (P1 pin 31), HLB1 (P1 pin 32) and HLB2 (P1 pin 33): Give latched band information decoded by U16 to control Q13, Q14, Q15, and Q16 in Block D, to generate the HET signal which controls Q17 in Block H, and to generate the LO Band and HI Band signals which control Q11 and Q18 in Block E.

HENDKICK: (U12B pin 6 Block I) A signal that is HIGH when both the SYTM and YO kick pulses are OFF and it is routed to the A24 Attenuator Driver board to be read by the processor. If HENDKICK remains LOW for more than 90 msec the processor ignores it and activates the fault light indicating a KICK error.

U17, U18, and U19 are open collector quad comparators used to drive all of the FET switches on the board (except Q3, Q21 and Q25). The inputs to the FETs are TTL level signals. The outputs are pulled to -15V for low output and pulled up to the level set by the pullup resistor connected to the individual comparators. R93 and R94 set the switching threshold of 1.3V for the comparators.

Kick Pulses J

In order to set up a uniform past history for each sweep and to force the SYTM to settle faster, a sequence of kick pulses is used at the end of each sweep with a start frequency less than 22.5 GHz. Sweeps with start frequencies greater than 22.5 GHz are not kicked. When kicked, the STYM is kicked positive in frequency until a predetermined current is reached, then the SYTM is kicked negative in frequency until a second predetermined current is reached, it then is allowed to settle from that point. The kick pulses minimize the differences between the various sweep conditions (continuous, line, external, single, and alternate). They are not needed at bandcrossings because the SYTM's past history at bandcrossings is similar to that provided by the kick pulses.

When Q21 and Q25 in Block H are both open the base current to the triple darlington is removed and the drive current decays to zero current resulting in a negative (in frequency) kick pulse. With Q25 open and Q21 closed the driver saturates and the current heads towards its maximum steady-state value giving a positive kick pulse.

The frequency to which the SYTM is tuned is proportional to the current through the SYTM coil. The current through the coil is sensed by sensing the voltage on the sense resistor (at P1 pin 44). This voltage is compared with adjustable preset levels by the two comparators (U7, U23) that drive Q21 and Q25.

It is necessary to deactivate the comparators when kick pulses are not desired so they don't interfere with the normal tuning of the SYTM. LM311's were chosen for the comparators because of the strobe pin that allows the comparators to be deactivated. In the deactivated state, the comparators will have a high output. Normal operation of the current driver requires Q25 to be an n-channel FET (normally ON) and Q21 to be a p-channel FET (normally OFF). The outputs of the comparators are used in the control of the strobe. The comparators are deactivated when 3 to 5mA of current is drawn out of pin 6. Hence, U23 is deactivated when Q24A is turned ON. Likewise, U7 is deactivated when Q19A is turned ON. Q19B and Q24B are used as current mirrors with the necessary gain to insure that Q19A and Q24A have 3 to 5mA in the OFF state. R114 and R82 set the current ratio between Q19A and Q19B. R115 and R108 set the ratio between Q24A and Q24B.

Q21 is turned OFF when the gate voltage is more positive than -11V but the gate voltage shouldn't exceed +15V due to a 30 volt Vgs breakdown specification for Q21. When the comparator is in the HIGH state R81 pulls the comparator output up to +5.2V. R83 feeds this level into the base of Q19A to latch the comparator into the HIGH state. In order for the comparator to become active Q19A must be turned OFF. This is accomplished by pulling the base

voltage down below 0.6V. When the kick pulse is desired, Q20 is momentarily turned ON which pulls the voltage down at the base of Q19A turning Q19A OFF and thus activating the comparator. If the voltage on the sense resistor is more positive than the voltage set by R10, the output of comparator U7 will go LOW (-15V) turning Q21 ON and keeping Q19A OFF. CR8 keeps the output of U7 from pulling the base of Q19A below -0.4V. The comparator remains in this state until the voltage on the sense resistor reaches the threshold set by R10. The output of the comparator then switches to +5.2V turning Q21 OFF and Q19A ON which latches the comparator into the HIGH state until Q20 is again pulsed ON.

Q25 is turned OFF when the gate voltage goes to -15V and turned ON when the voltage is pulled up to the level of Q25's source voltage. U23 has an open collector output so the gate of Q25 is pulled up to the same voltage as the source by R103 in Block H. Again the the output of the comparator (U23) is used to latch itself into its HIGH state. In order to activate U23, Q24A must be turned OFF. This is accomplished by pulsing Q23 ON. The comparator then switches to its active mode and if the voltage sensed at the sense resistor is more negative than the level set by R9, the output of the comparator goes to -15V which turns Q25 OFF and turns Q22 ON. When Q22 is ON it keeps U23 in the active mode by keeping Q24A OFF. CR9 keeps Q22 from pulling the base of Q24A below -0.4V. The 11 volt zener (VR1 in Block H) insures that the output of the op amp won't go negative enough to turn Q22 OFF when the comparator is in the LOW state. R102 is chosen in conjuntion with the 11 volt zener to insure that Q22 will be able to pull the base of Q24A to 0 volts.

Thus, when a kick pulse trigger (KICK T) is sent by the microprocessor (by setting the common point of R107 and R104 to a HIGH TTL logic level) both comparators are activated and Q25 is turned OFF while Q21 is turned ON (R9 and R10 are adjusted to levels out of the normal SYTM operating range). Q21 remains ON causing the current to the coil to increase until the threshold set by R10 is reached. U7 then turns Q21 OFF and latches in this state. The coil current then decreases until the threshold set by R9 is reached. U23 then turns Q25 ON and latches in this state. Both comparators remain in their latched state until another trigger pulse is sent. U23 is in it's active mode during both kick pulses. LYTMKICK is a TTL level signal that is LOW when Q24A is OFF indicating when the kick pulses are active. LYTMKICK (offset by a diode drop) is also used to switch out the compensation during the kick pulses (see section G). If the compensation were left in it would be able to interfere with the current sense level to the extent that the negative kick pulse wouldn't shut OFF.

Voltage Reference K

The +10 VREF and -10 VREF are generated for cases where accurate supply voltages are needed. The +10V reference is adjusted by R85 to null the offset error in Band 0 of the +1.0/+0.5 V/GHz lines (see Block F). It has a maximum temperature drift of 25 ppm/degrees C. R84 is used to reduce the loading on the +10V reference (U5). U13, R86, R87 and R88 form a voltage inverter creating a -10V reference supply.

Power Supplies L

The power supplies coming to the board are: the +20V supply (P1 pins 1 and 23), the +5.2V supply (P1 pins 2 and 24), the -10V supply (P1 pins 3 and 25), the -15V supply (P1 pin 4) and the -40V supply (P1 pins 5 and 27). All supplies coming onto the board (except the -40V supply) are filtered by low-pass filters consisting of a 4.7uH inductor in series with the supply followed by a 1uF capacitor shunting across the supply to power ground. The -40V supply (P1 pins 5 and 27) is used as a reference voltage in block H (Current Driver) and is not shown in block L of the schematic.

U11 regulates the +20V supply and provides a +15V supply to the rest of the board.

TROUBLESHOOTING PROCEDURE

NOTE

Perform the following tests shown in Roman numerals. If one of the steps fail, perform the associated substeps shown in uppercase alpha characters. If one of the steps in uppercase alpha characters fail, perform the associated substeps shown in numeric characters.

I. Check the voltages on the power supplies. P1 Pins 1,23 should be +20V +-0.2V, P1 Pins 2,24 should be +5.2V +-0.05V, P1 Pins 3,25 should be -10V +-0.1V, P1 Pin 4 should be -15V +-0.2V, P1 Pins 5,27 should be -40V +-.7V, U9 Pin 6 should about +10V adjustable by R85 and U10 pin 6 should be the negative of U9 Pin 6 +-1.3mV.

II. Set 8340A to CW 10MHz and adjust R85 (Block K) until the voltage out of the +1.0 V/GHz backpanel connector reads 10mV +-1.5mV.

A. If +1.0 V/GHz line won't adjust to 10mV at 10MHz then check U9 pin 6. Output should vary around +10V as R85 is varied.

B. Check the -0.25 V/GHz line, R85 should be able to adjust it to 2.5mV +-0.05mV. If OK then check P1 Pin 17, it should read 10mV +-1.5mV when adjusted by R85. If it is correct at P1 Pin 17 then the rear panel BNC isn't connected to the +1.0 V/GHz line.

1. R41 (Block F) should have about 5V across it.

2. U8 (Block F) shouldn't be saturated.

3. R38 should have less than 0.4V across it. If R38 has 0.4V or more, check the +1.0 V/GHz line for an output short.

C. Check PRETUNE line at P1 Pin 22. It should read -9.25V +-4mV.

1. Pull out A28 SYTM driver board and verify that the PRETUNE line is valid on the A54 YO Pretune board (TP3). Troubleshoot or adjust as necessary.

D. The gate of Q11 should have the same voltage as U6 pin 6 and the gate of Q18 should be about -15V.

1. U16 Pin 13 (Block I) should be LOW. U16 Pins 12, 11, and 10 should be HIGH.

a. U16 pins 1 and 3 should be LOW. U16 Pin 2 should be HIGH. If not, pull out SYTM driver board and verify the latched band information on the A27 Level Control board; otherwise replace U16.

E. The gate of Q5 should have the same voltage as U7 pin 6.

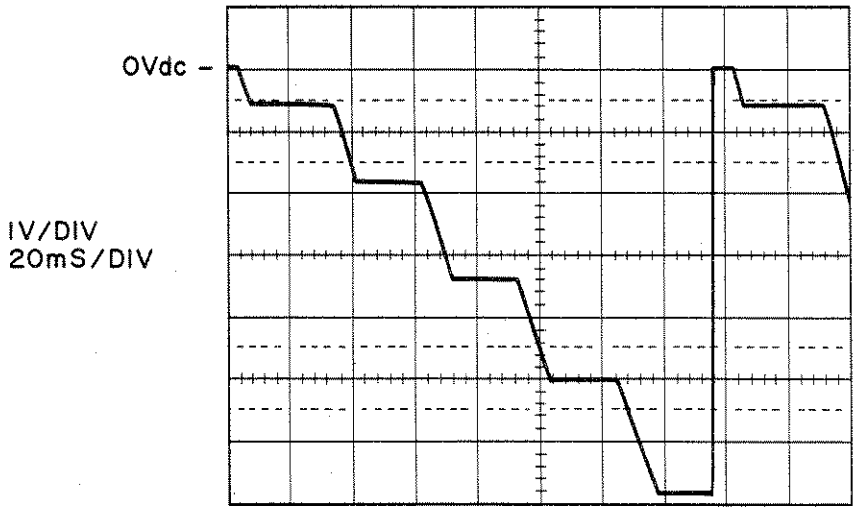
1. U14 Pin 1 should be low, it is an input to a three input and gate whose output U14 Pin 12 should also be low.

a. If U14 Pin 1 isn't low check latch U15 for correct
a. If U12 Pin 1 (Block I) isn't LOW check latch U13 for correct operation
by using the signature analyzer test described Assembly. IO channel 11 subchannel 3 is the address of the strobe used with U15. This test may also be done the strobe used with U13. This test may also be done 'SHIFT GHz 11 Hz SHIFT MHz 3 Hz SHIFT KHz 8 Hz'. U15 'SHIFT GHz 11 Hz, SHIFT MHz 3 Hz, SHIFT KHz 8 Hz'. U13 Pin 2 should be HIGH. Then enter '65527 Hz' U13 Pin 2 should now be LOW. If either condition fails, it indicates a problem with either the Data Bus or U13.

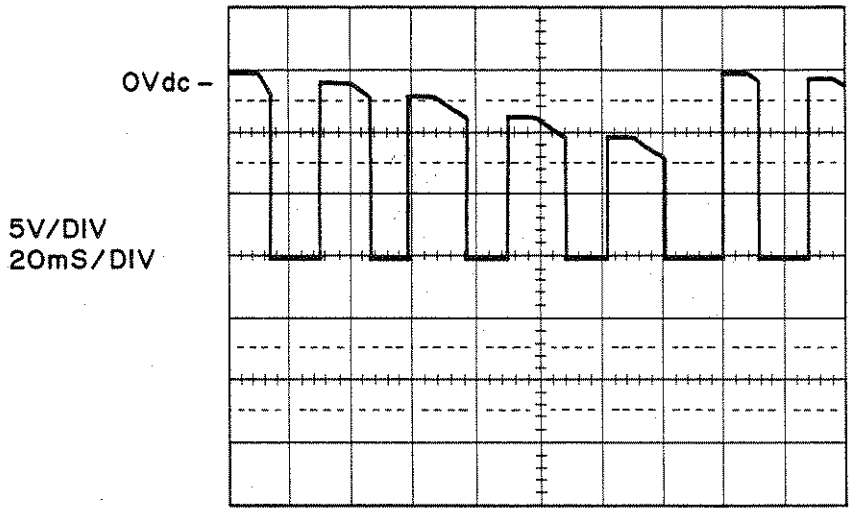
III. Connect voltmeter rear panel to +1.0 V/GHz BNC. It should vary with the instrument frequency up to about 19V. Check test point A28 TP4 labeled V/GHz to verify correct operation. The voltage at TP4 should read -0.25 v/GHz times the instrument frequency. The voltage readings should be within the following limits at room temperature:

Frequency	-0.25 V/GHz	+1.0 V/GHz
2.2 GHz	+-4mV	+-22mV
5 GHz	+-3mV	+-25mV
10 GHz	+-4mV	+-34mV
15 GHz	+-5mV	+-52mV
18 GHz	+-5mV	+-58mV
22 GHz	+-6mV	
26 GHz	+-6mV	

Check the waveform at TP4 (V/GHz) during a full-band sweep. There should be no discontinuities during a bandswitch. It should look like:



A. Check the voltage at the gate of Q5 during the sweep, it should have the the following waveform:



B. Check PRETUNE line at P1 Pin 22. It should read -2.5 v/GHz (relative to YO frequency).

1. Pull out A28 SYTM driver board and verify that the PRETUNE line is valid on the A54 YO Pretune board (TP3). Troubleshoot or align where necessary.

C. In CW operation, the gate of Q12 (Block H) should be at -15V. In band 0, Q11 should be at the same level as U6 pin 6 while Q13, Q14, Q15, Q16 and Q18 should be at -15V. In band 1, Q15 and Q18 should be at the same level as U6 pin 6 while Q11, Q13, Q14 and Q16 should be at -15V. In band 2, Q16 and Q18 should be at the same level as U6 pin 6 while Q11, Q13, Q14 and Q15 should be at -15V. In band 3, Q13 and Q18 should be at the same level as U6 pin 6 while Q11, Q14, Q15 and Q16 are at -15V. In band 4, Q14 and Q18 should be at the same level as U6 pin 6 while Q11, Q13, Q15 and Q16 are at -15V.

1. Check latched band information on U16 (Block I) Pins 1, 2 and 3 (P1 Pins 31, 32 and 33). Pin 1 should be HIGH in bands 0, 2 and 4 and LOW in bands 1 and 3. Pin 2 should be HIGH in bands 1 and 2 and LOW in the other bands. Pin 3 should be HIGH in bands 3 and 4 and LOW in the other bands.

2. Pull out SYTM driver board and verify the latched band information on the A27 Level Control board.

3. Verify U16, all outputs should be high except for pin 14 in band 0, pin 13 in band 1, pin 12 in band 2, pin 11 in band 3 and pin 10 in band 4.

D. Check U22 (Block H) to see if it is saturated. If saturated the voltages on pins 2 and 3 will differ. Since there is input diode protection, current will shunt along the input path through the programmable scaler causing an error voltage to be added to the V/GHz lines.

1. Measure the voltage at A28 TP 5 labeled "SRS" to determine the current flowing through the SYTM coil. If the voltage is around 8V or more. the SYTM output current drive is saturated. Check for collector to emitter shorts in Q26 , Q27 and the drive transistor A47Q2 on the sense resistor bracket. If the drive transistor is shorted the same voltage that appeared on the "SRS" test point should appear on A62XA28 Pin 20 with the A28 SYTM driver removed. Also verify that the gate of Q21 is at +5V in CW operation.

2. If the output of U22 is against the negative supply rail check to make sure that Q25 is on during CW operation.

a. Measure the base-emitter voltages of Q26, Q27 and the drive transistor. Replace the trasnsitors that have abnormal base-emitter voltages. Normal base-emitter voltages should be about -0.6V.

E. Check U6 (Block E), U5B and Q6 if still having problems with the -0.25 V/GHz line.

IV. Look at the waveform at TP 5 labeled "SRS" during a sweep.
R9 (Block J) should adjust the height of the negative kick pulse (about -9V),
R10 should adjust the depth of the positive kick pulse (about 0V),
and R8 (Block H) should adjust the overall amplitude of the waveform.

A. Check the emitters of Q24A and Q19A to verify that the pulse trigger is reaching that point.

1. If no kick pulses are present check pin 7 of U13 (Block I) for a positive trigger pulse.

B. Check the inputs and ouputs of U23 and U7 to see if they become active at all.

C. If only a positive kick pulse is present, check P1 Pin 42 (SYTM COIL+). The voltage should drop to -125V +-7V. If it drops to about -140V it means that the diode on the SYTM bias board is clamping the coil voltage. Check VR2 and CR11 in Block H. If it drops less, the zener diode on the SYTM bias board may be breaking down at too low a voltage.

V. Look at TP1 "CMP" (Block G) and verify that R1 (Block A), R2, R3, R4 and R5 (Block C) can affect output at 26.5 GHz. Verify that U4 (Block C) and R1 (Block A) can both increase and decrease the compensation.

VI. Look at the voltage across C26 (TP2 Block B) during sweep. It should look like a ramp with an offset. The knee should be rounded. This waveform should restart at each bandcrossing. The overall amplitude should vary with sweep time. R6 (DVO) should vary the height of the knee and R7 (DVS Block B) should vary the slope of the ramp.

A. If there is no signal check Q9, it should be gated by HSP via U18 pin 14. Check U2 pin 10 and U2A pin 1.

B. If there is no slope, or if the slope doesn't reset at bandcrossings, check Q10 (gated by HSP via U18 pin 1). Also check U5A pin 1.

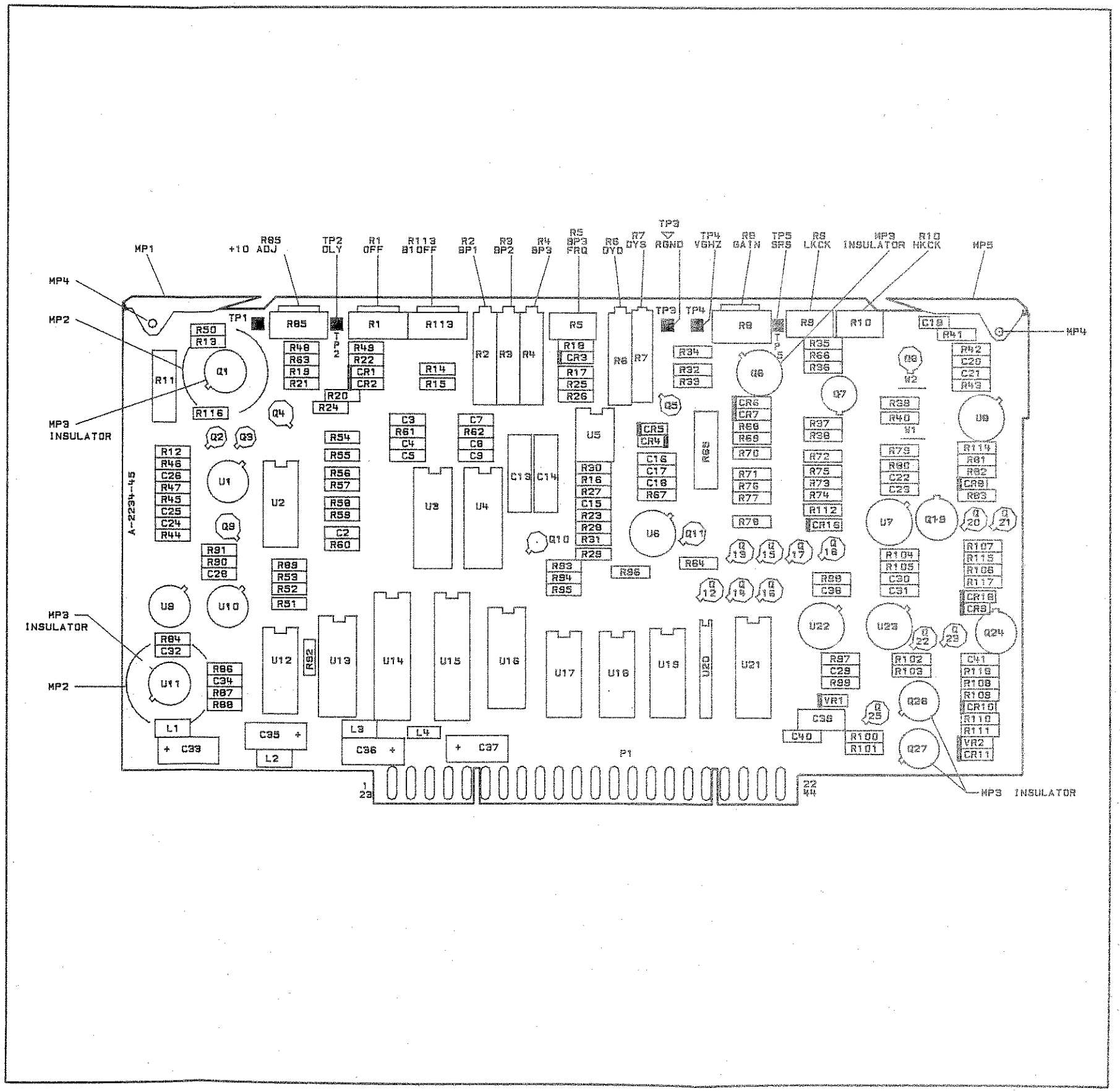


Figure 8-667. A28 SYTM Driver, Component Location Diagram

TP4

DRIVER 25

Ⓐ OFFSET COMPENSATION

+10VREF
R1 10K
OFF
CW
-10VREF
R19 75K
Q4
R24 46.4K
R49 3000
B2OFF
R63 50K
R113 10K
CW
R48 3000
+10VREF

Ⓑ DELAY COMPENSATION

(10, R2:) P1-29 (W) W BAND

-.25V/GHz

R28 2000
295 46.4K
R31 2000
Q10
R23 10K
C13 .033
+15VF
U5A
C15 0.1
-15VF
R29 10K
DYS
CW
R7 3000
R26 2370
+15VF
U2A
-20VF
C2 0.1
-15VF
R55 2500
R25 26.1K
R54 10K
DYO
R6 50K
-10VREF

U14 +5.2VF
C3 0.1
+15VR
U3
REG
DB3 DB4 DB5 DB6 DB7 DB8 DB9 DB10
[LOAD] [DATA] [MSB] [LOCK TRANSFER]
DAC 8
[V HIGH] [V LOW] [COMM] [I+] [I-]
R4 2500
C5 100pF
-15VF
C4 0.1
-15VR
5V

I DLY RES

I B2OFF

8/
8/
3/

DB3 DB4 DB5 DB6 DB7 DB8 DB9 DB10

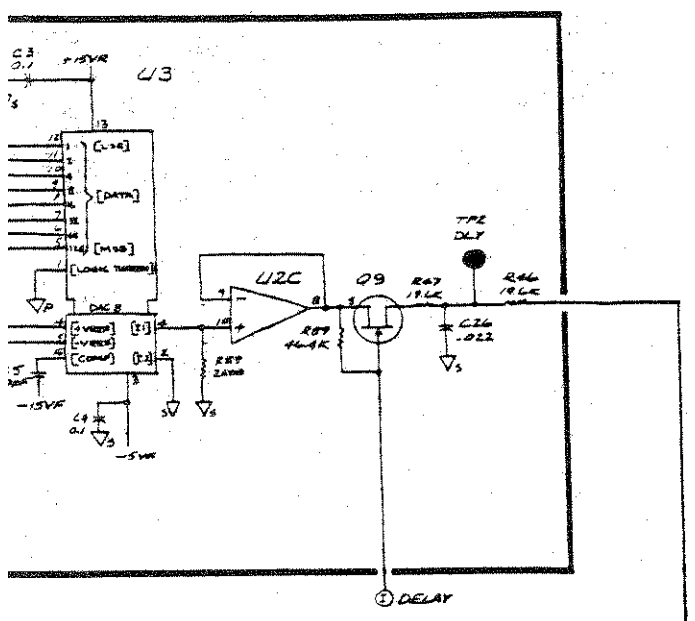
Ⓔ -0.25V/GHZ

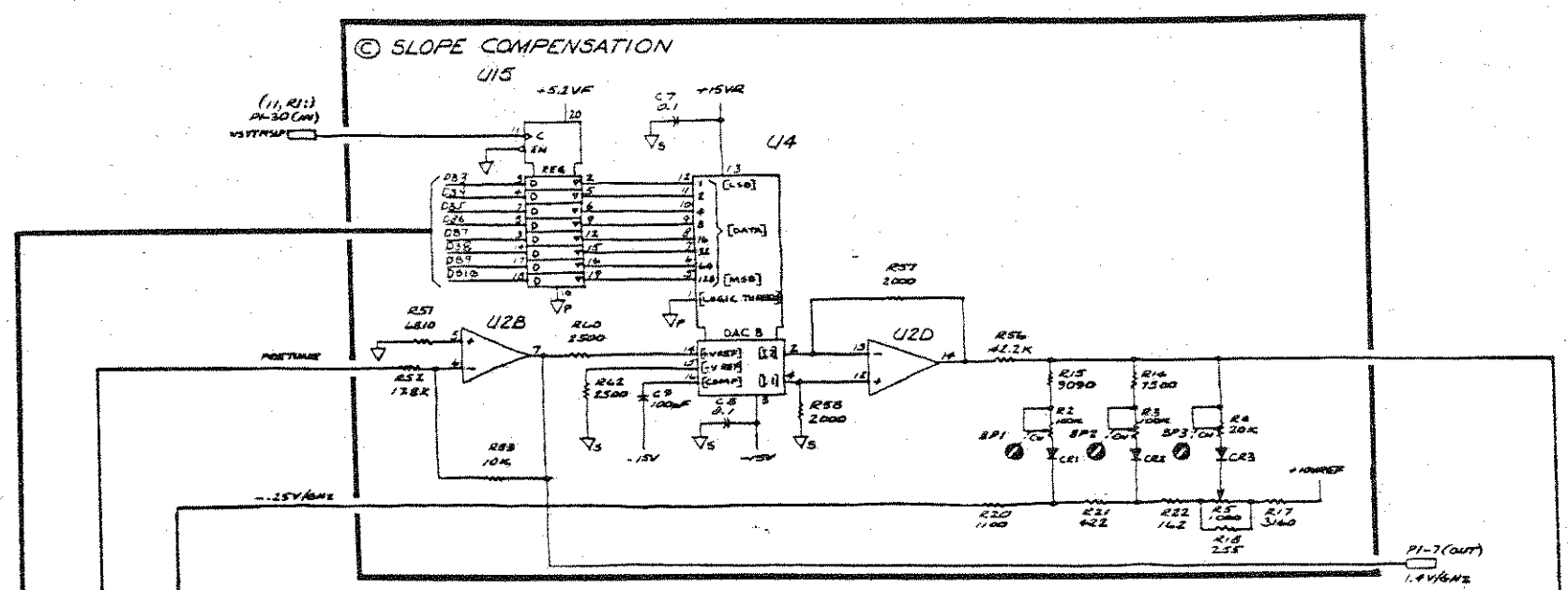
+10VF
TP6 VGHI (-0.25V/GHz)
R27 10K
R32 5110
+10VR
+10VF

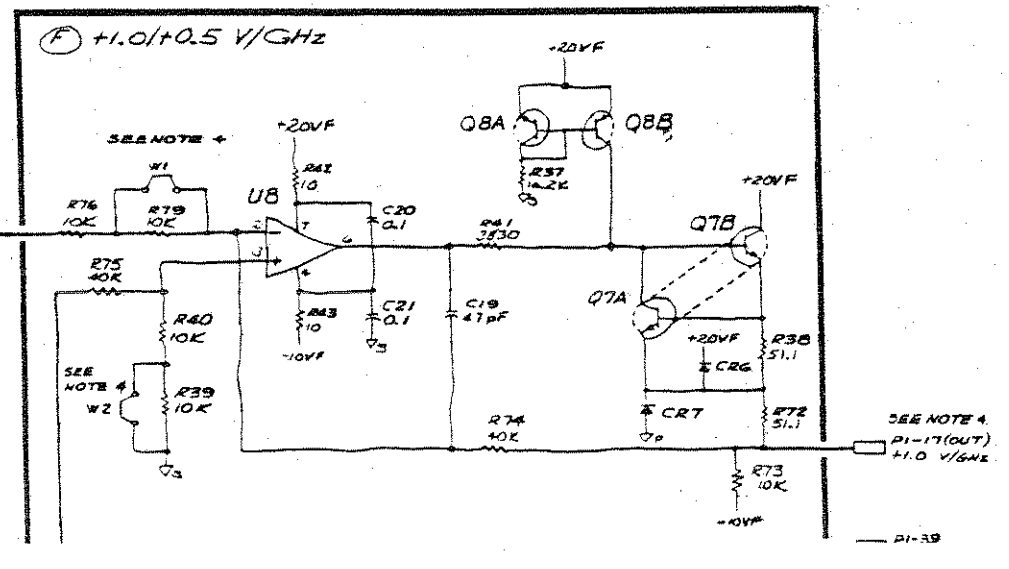
TP2

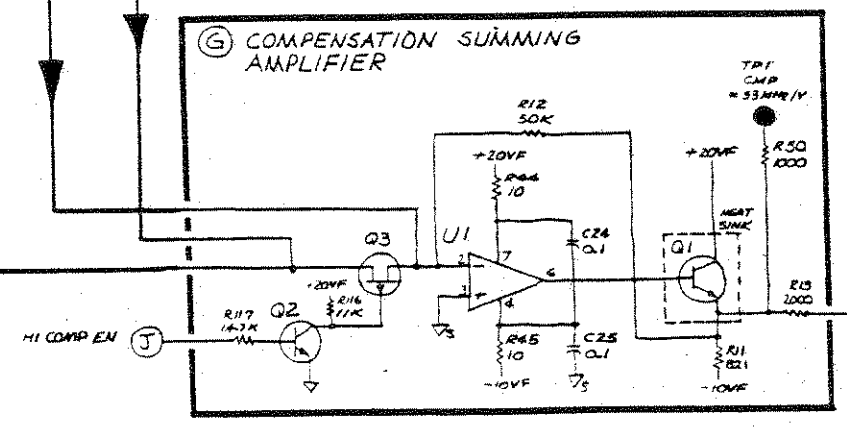
TP1

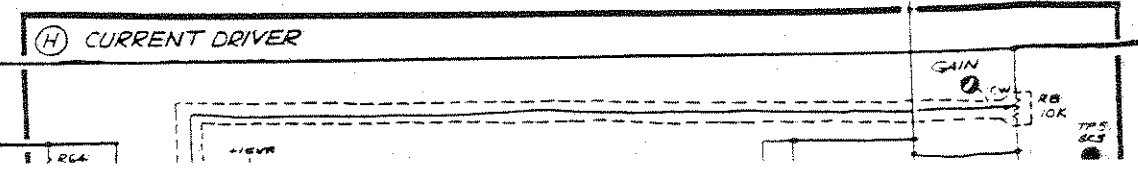
TP5

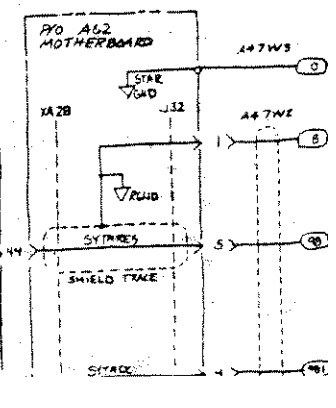

U3
+15VR
[D-to-A]
[DATA]
[MSB]
[LOGIC THRESH]
DAC B
[V REF]
[COMP]
U2C
09
R67
19.1K
R66
19.1K
TP6
DLY
R69
44.8K
C26
.022
R68
2490
-15VF
-5VR
DELAY


© SLOPE COMPENSATION
U15
+5.2VF
(11, R13) PA-30 (W)
VSYTRSUP
C7
.1
+15VR
U4
REG
DB3
DB4
DB5
DB6
DB7
DB8
DB9
DB10
[D-to-A]
[DATA]
[MSB]
[LOGIC THRESH]
DAC B
[V REF]
[COMP]
R51
1.810
U2B
R52
137K
R49
2.500
R48
2.500
C9
.100mF
C8
.1
R58
2.000
R57
2000
U2D
R56
44.2K
R53
104
-15V
-5V
R15
9090
R14
7500
R1
100K
R2
100K
R3
100K
R4
20K
SP1
SP2
SP3
CR1
CR2
CR3
+10VREF
R20
1.00
R21
422
R22
162
R5
100K
R16
255
R17
3.40
P1-7 (OUT)
1.4 V/GHz
-.25V/GHz


(F) +1.0/+0.5 V/GHz
+20VF
SEE NOTE 4
W1
R76
10K
R79
10K
U8
R42
10
C20
.1
R41
3830
Q8A
Q8B
R37
14.2K
Q7B
Q7A
R75
40K
R40
10K
R43
10
C21
.1
C19
47pF
P38
51.1
CR6
CR7
R72
51.1
SEE NOTE 4
W2
R39
10K
R74
40K
R73
10K
-10VF
SEE NOTE 4.
P1-17 (OUT)
+1.0 V/GHz
P1-39
P1-40 (OUT)
-.25 V/GHz


(G) COMPENSATION SUMMING AMPLIFIER
TP1
GAIN
.53MV/V
R12
50K
+20VF
R44
10
U1
C24
.1
Q3
Q1
HEAT SINK
R50
1000
R13
1000
R117
14.7K
Q2
R116
7.11K
HI COMP EN
J
R45
10
C25
.1
R11
821
-10VF


(H) CURRENT DRIVER
GAIN
R8
10K
+15VR


P/O A62 MOTHERBOARD
A47W3
A47W2
XA28
J32
STAR GND
PLUG
SYTRES
SHIELD TRACE
SYTRSUP

TP5

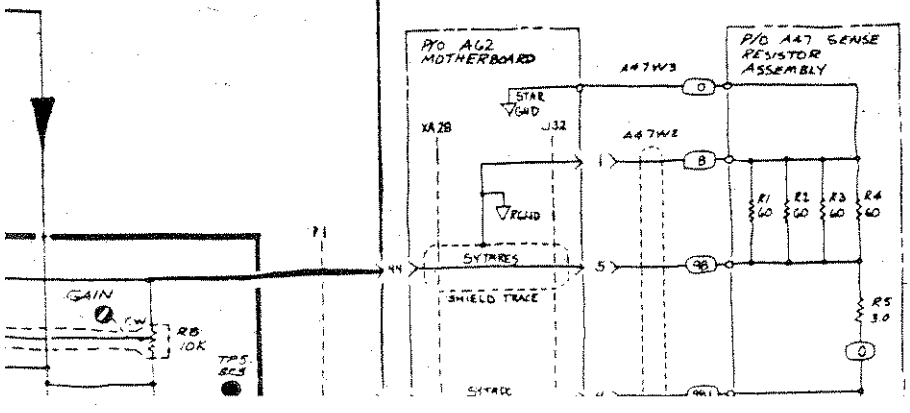
NOTES:

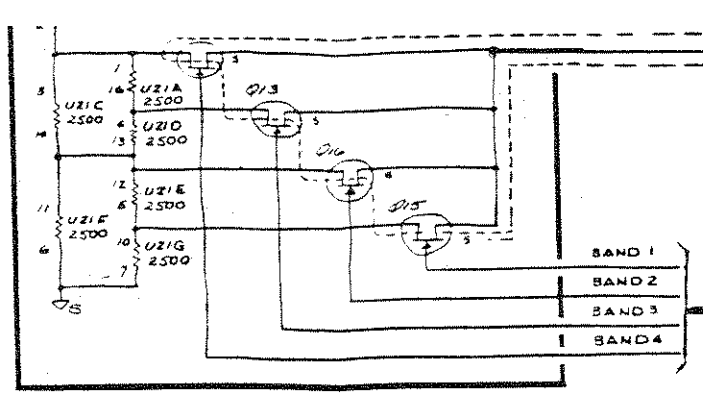
1. REFER TO FIGURE 8-X FOR DETAILED SCHEMATIC DIAGRAM SYMBOLOGY NOTES.

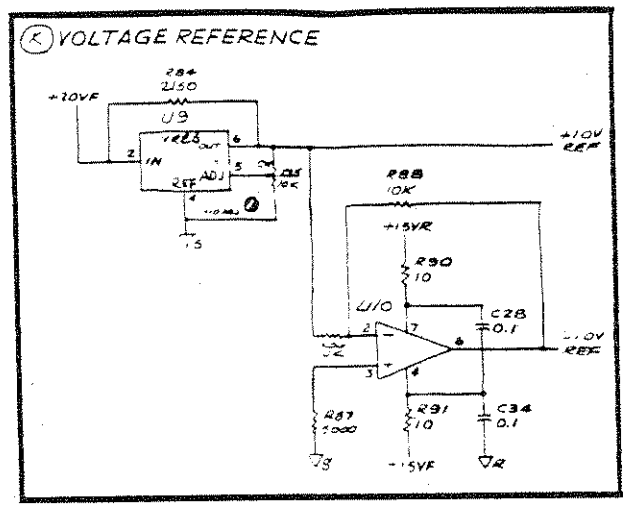
2. RESISTANCE VALUES SHOWN ARE IN OHMS, CAPACITANCE IN MICROFARADS, AND INDUCTANCE IN MICROHENRIES UNLESS OTHERWISE NOTED.

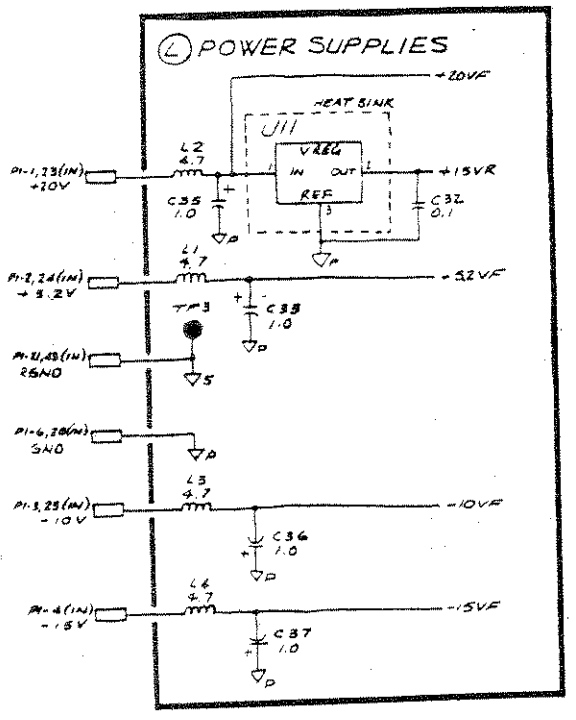
3 THE A47 SENSE RESISTER ASSEMBLY IS CONNECTED TO GROUND ON THE A62 MOTHERBOARD ASSEMBLY BY ITS MOUNTING HARDWARE.

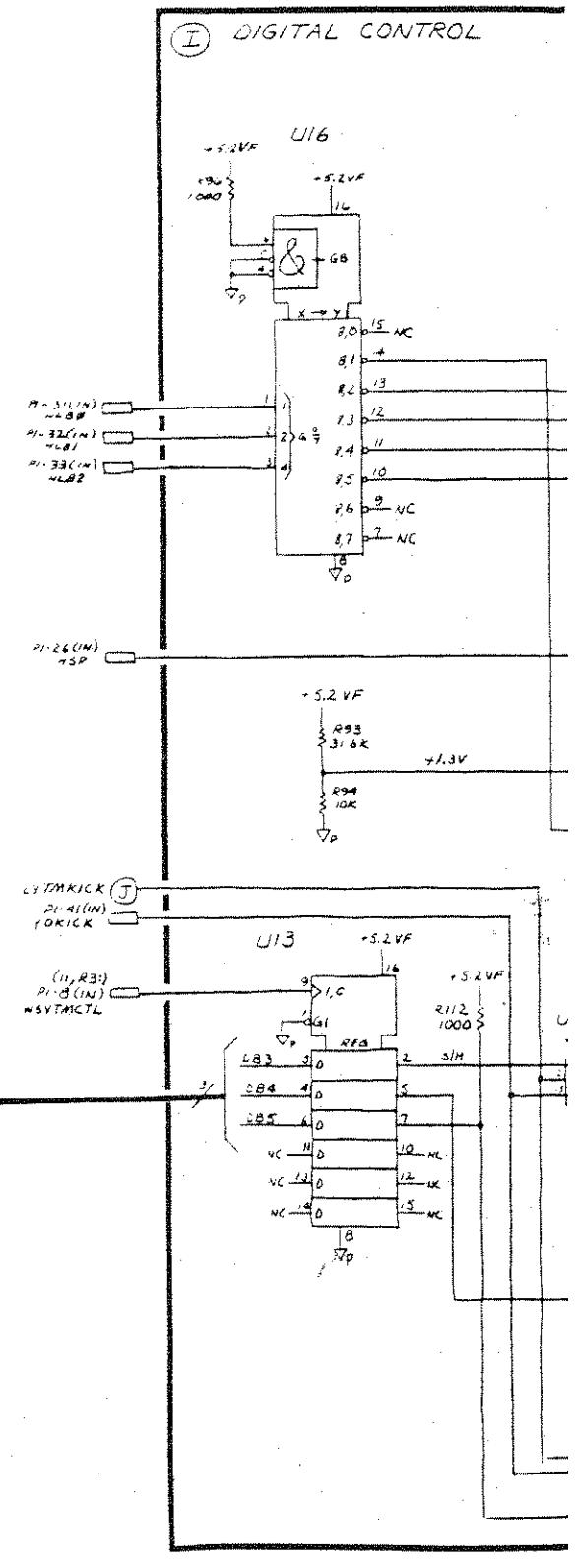
4 THE VOLTAGE SENSITIVITY OF THIS LINE IS PRESET TO +1.0V/GHZ LIMITING AT 19 VOLTS. IN ORDER TO COVER THE ENTIRE FREQUENCY RANGE OF THE 8340, JUMPERS W1 AND W2 MAY BE CUT. THAT WILL CHANGE THE SENSITIVITY TO +.5V/GHz.











SERIAL PREFIX: A-2234-45 4 OCT. 82

CONTROL

U20 46.4K

U19A +5.2VF -15VF

U19D

U19B

U19C

BAND 1

BAND 2

BAND 3

BAND 4

15 NC 13 12 11 10 9 VC 7 NC

U18C

U18B

U18D

U18A

+1.5V

(E) PULL UP

(B) DELAY

(B) DLY RES

(E) BAND 1-4

(E) BAND Ø

+5.2VF R112 1000

U12A

3/M

U17D

U17C

U17A

U17B

(A) BIOFF

(H) MET

(E) SAMPLE

(H) SYTM SEL

+5.2VF R92 1000

U12B

21-13 (OUT) MENUKICK

HET (T)

Q17 -15VF

R78 46.4K

R77 2150

R71 19.6K -10VF

C29 0.1

R97 10

VR1 11V

R103 31.6K

Q21 -15VF

R109 5110

VR2 100V

CR11

R100 1000

R101 28.1K

C39 .0027

C40 330pF

42

SYTM COIL +

ASTHERBOARD GROUND PLANE

NOTE 3

P/O J18

P/O J483

5, 27

-10V

(J) KICK PULSE

+15VR R105 10

R34 147

LKCK

U23

R9 1000 CW

R35 11.5K

C30 0.1

C31 0.1

R102 1000

-5.2VF R106 2610

Q22

Q24A Q24B

(I) LYT/MKICK

(G) HI COMP EN

CR10

R108 422

R115 2.4K

CR9

Q23

CURRENT SENSE

KICK TRIGGER

CR16

R107 31.6K

KICK TO LOW FREQUENCY CURRENT CONTROL

KICK TO HIGH FREQUENCY CURRENT CONTROL

+15VR R80 10

U7

MKCK

R10 10K CW

R66 14.7K

R36 7900

-10V REF

C22 0.1

C25 0.1

R81 10K

R83 7500

Q19A Q19B

R82 162

R114 3160

R104 31.6K

Q20

CR8

-0.25 V/GMZ GUARD TRACE

Q25 Q26

SYTMSB

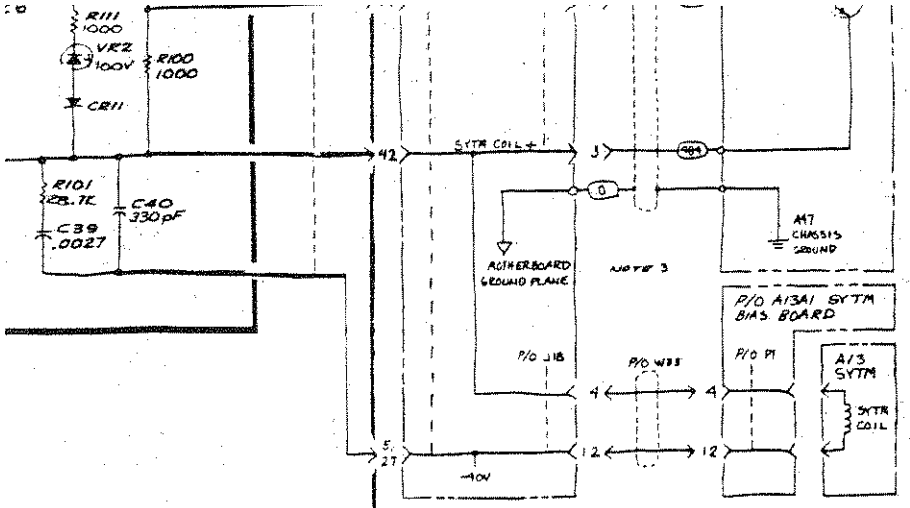


Figure 8-670. A28 SYTM Driver, Schematic Diagram

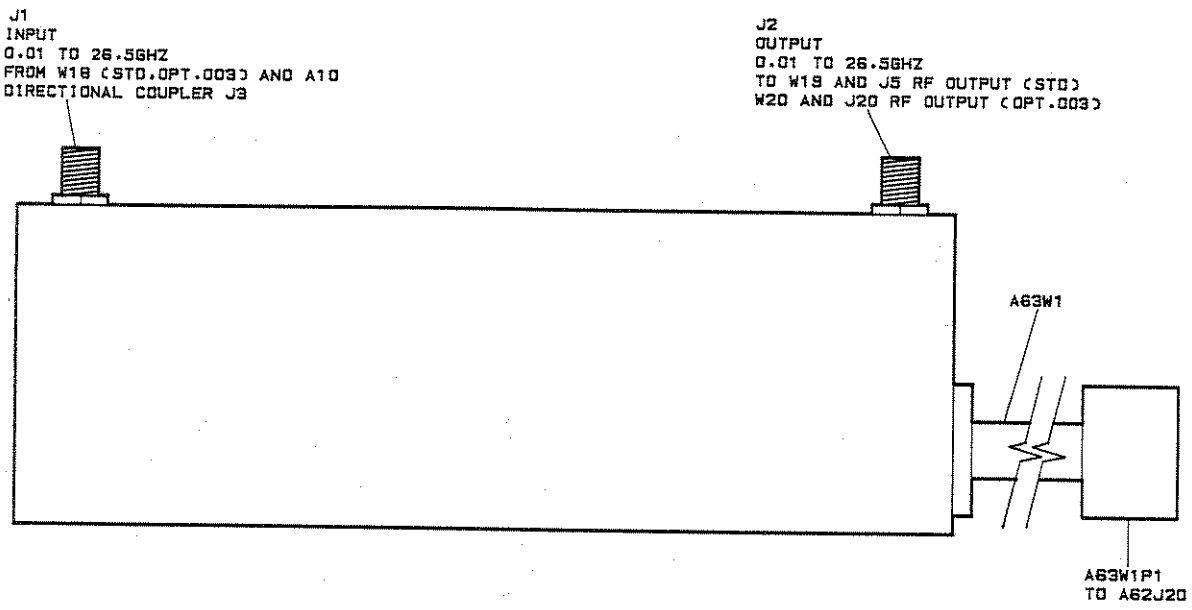


Figure 8-674 A63 70 dB Programmable RF Attenuator, Component Location Diagram

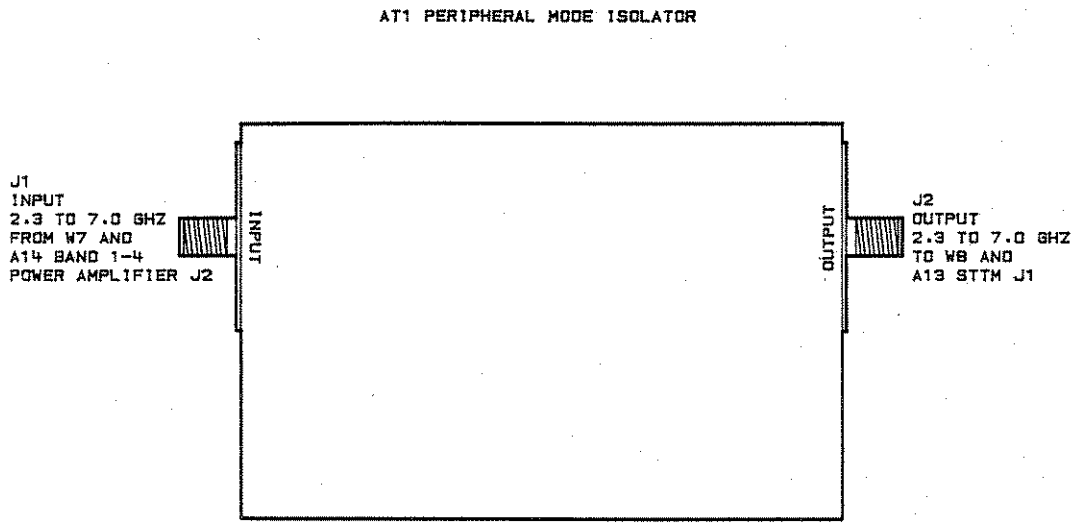
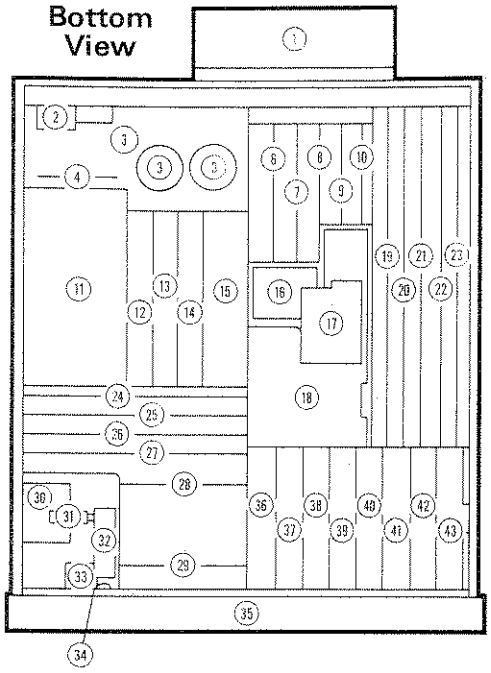
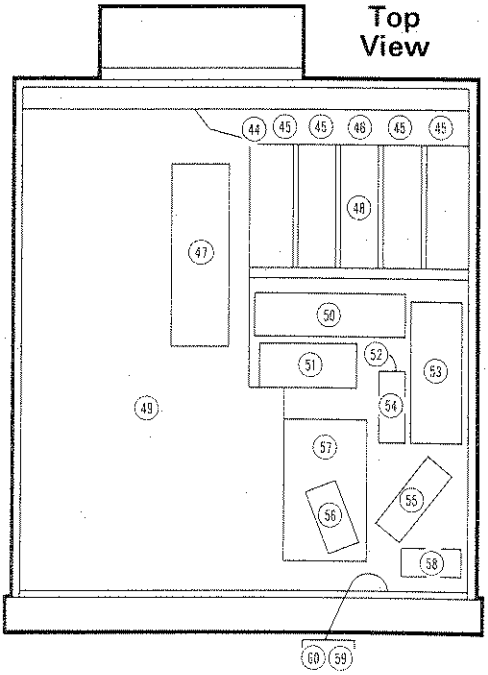


Figure 8-677A. AT1 Peripheral Mode Isolator, Component Location Diagram

REFERENCE GUIDE TO SERVICE DOCUMENTATION





Assy./Ref. Des.	Description	Location	Volume 2					Volume 3		
			Ref.-M/N Loops	20/30 Loops	Swp. Gen.-YO Loop	Motherboard	Controller	Front/Rear Panel	RF Section	Power Supplies
A1	Alpha Display	35					●			
A2	Display Driver	35					●			
A3	Display Processor	35					●			
A4	Not Assigned	-								
A5	Keyboard	35					●			
A6	Keyboard Interface	35					●			
A7	Lower Keyboard	35					●			
A8	3.7 GHz Oscillator	51						●		
A9	Band 0 Pulse Modulator	56						●		
A10	Directional Coupler	32						●		
A11	Band 1-4 Detector	31						●		
A12	Band 0 Detector	34						●		
A13	SYTM (Switched YIG Tuned Multiplier)	30						●		
A14	Band 1-4 Power Amplifier	53						●		
A15	Band 0 Low Pass Filter	52						●		
A16	Band 1-4 Modulator/Splitter	51						●		
A17	Band 0 Mixer	54						●		
A18	Band 0 Power Amplifier	55						●		
A18A2	Band 0 Splitter	60						●		
A19	Capacitor Assembly	48								●
A20	RF Section Filter	50						●		
A21	Pulse Modulator Driver	29						●		
A22	Not Assigned	-								
A23	Not Assigned	-								
A24	Attenuator Driver/SRD Bias	28						●		
A25	ALC Detector	27						●		
A26	Linear Modulator	26						●		
A27	Level Control	25						●		
A28	SYTM Driver	24						●		
A29	Reference Phase Detector	12	●							
A30	100 MHz VCXO (Voltage Controlled Crystal Osc.)	13	●							
A31	M/N Phase Detector	4	●							
A32	M/N VCO (Voltage Controlled Osc.)	15	●							
A33	M/N Output	15	●							
A34	Reference-M/N Motherboard	5	●							
A35	Rectifier	4								●
A36	PLL1 VCO (Voltage Controlled Osc.)	36		●						
A37	PLL1 Divider	37		●						
A38	PLL1 IF	38		●						
A39	PLL3 Upconverter	39		●						
A40	PLL2 VCO (Voltage Controlled Osc.)	40		●						
A41	PLL2 Phase Detector	41		●						
A42	PLL2 Divider	42		●						
A43	PLL2 Discriminator	43		●						
A44	YIG Oscillator (YO)	10			●					
A45	Pre-Leveler	10			●					
A46	7 GHz Low Pass Filter	10			●					
A47	Sense Resistor Assembly (YO circuit)	47			●					
	(STYM circuit)	47						●		
A48	YO Loop Sampler	18			●					
A49	YO Loop Phase/Detector	18			●					
A50	YO Loop Interconnect	17			●					
A51	Reference Oscillator	16	●							
A52	Positive Resulator	6								●
A53	Negative Regulator	7								●
A54	YO Pretune DAC/Delay Compensation	8			●					
A55	YO Driver	9			●					
A56	-15V Regulator	10								●
A57	Marker/Bandcross	19				●				
A58	Sweep Generator	20			●					
A59	Digital Interface	21				●				
A60	Processor	22				●				
A61	Memory	23				●				
A62	Main Motherboard	49					●			
A63	70 dB RF Attenuator	58						●		
AT1	Peripheral Mode Isolator	58						●		
B1	Fan Assembly	1								●
A62C1-3	Power Supply Filter Capacitors	3								●
FL1	AC Line Module	2								●
A62Q1-4	Power Supply Regulating Transistors	2								●
A62S1	Power Supply Thermal Switch	44								●
T1	Power Supply Transformer	11								●
A62U1	Power Supply Regulator	46								●

POWER SUPPLIES — FAN

POWER SUPPLY CIRCUIT DESCRIPTION

The power supply includes the A19 Capacitor Assembly, the A35 Rectifier Assembly, the A52 Positive Regulator Assembly, the A53 Negative Regulator Assembly, the A56 -15V Regulator Assembly, and several A62 Motherboard and chassis mounted components.

NOTE

These include series pass elements for the majority of the instrument power supplies.

* A19 CAPACITOR ASSEMBLY provides +20V unregulated and -10V unregulated.

* A35 RECTIFIER ASSEMBLY provides -40V unregulated, +5v unregulated, and +22V regulated.

* A52 POSITIVE REGULATOR provides +20V regulated, and +20V switched which is turned on by HSTD, +12 regulated and +5.2V regulated.

* A53 NEGATIVE REGULATOR provides -5.2V regulated, -10V regulated and -40V regulated.

* A56 -15V REGULATOR uses the -40V regulated output to develop a -15V supply.

The AC Primary circuit, the A19 Capacitor board, and the A35 Rectifier board are shown together on one schematic diagram. The A53 Negative Regulator and the A56 -15V Regulator are shown together on another schematic diagram. The A52 Positive Regulator is shown on a separate schematic diagram. The circuit description for each assembly is included with the associated schematic diagram.

Refer to Figure 8-682A 8340A Power Supply Logic Block Diagram for a visual presentation of the power supply configuration.

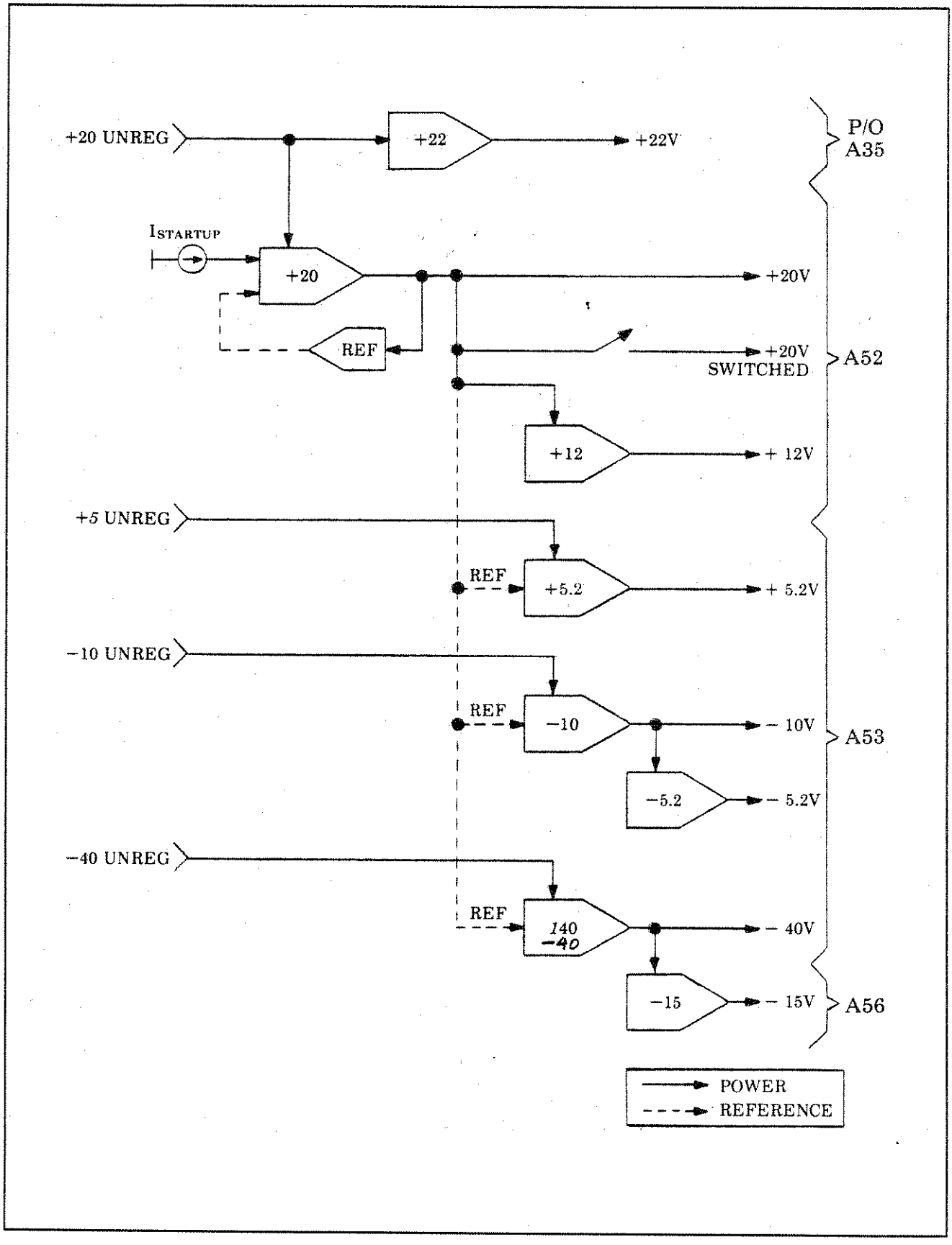


Figure 8-682A. Power Supply Logic Block Diagram

POWER SUPPLY CIRCUIT DESCRIPTION

Introduction

The power supply includes the A19 Capacitor Assembly, the A35 Rectifier Assembly, the A52 Positive Regulator Assembly, the A53 Negative Regulator Assembly, the A56 -15V Regulator Assembly, and several A62 Main Motherboard components (these include the pass elements for the majority of the instrument power supplies). Figure 8-682A is an overall block diagram of the power supplies. The +12V, +5.2V, -10V, and -40V power supplies are dependent upon the +20V supply with the -5.2V and -15V supplies being dependent upon the -10V and -40V supplies.

The main function of the Power Supply circuit is to produce the power supply voltages required for the 8340A. The circuit also generates the power-up flags HNUP, HPUP, and LIPS. These flags are used by the microprocessor and several other circuits to control instrument activity and to ensure proper initialization. Table 8-689A lists the signals received and generated by the power supply circuit and upon which boards they are located.

Table 8-689A. Power Supply Circuit Signals

To be supplied.

Primary Power

Primary power is supplied to the primary of T1 through Power Line Module FL1, which includes a line voltage selector PC board, and across C1 which filters audio noise. The voltage selector board is positioned to provide correct power connections to T1 for operation with line voltages of 100 VAC, 120 VAC, 220 VAC, or 240 VAC. Refer to Section II, Installation, in Volume 1 for complete instructions on the correct installation of the line voltage selection PC board.

Standby Mode

With line power connected and the front panel LINE switch in STANDBY, the following occurs. Power is supplied to the rectifiers on the A19 Capacitor and A35 Rectifier Assemblies. +20V unregulated is supplied to the +22V regulator on the A35 Rectifier Assembly and powers up that supply. The anode of DS1, front panel STANDBY LED, and the cathode of A62CR2 are grounded, which lights DS1 and reverse biases CR2. A62K1 switches into STANDBY (B1 remains OFF) and LSBY is sent to the +20V regulator

which keeps it OFF, along with the other regulators. Other LEDs that will be ON are A62DS1 (line power connected indicator), A16DS1 (power ON safety indicator) and A35DS1 (+22V regulator operational indicator).

NOTE

Although the +22V regulator is the only operational supply, line power is present, the rectifiers are fully operational and the filter capacitors are fully charged; care should therefore be taken when servicing the unit.

When switching the LINE switch from STANDBY to ON, A62K1 pin 1 goes to +22V, switching A62K1 into the ON position, thus energizing B1. Simultaneously, LSBY goes from 0V to +22V which allows the +20V regulator and other regulators to beome operational.

A19 CAPACITOR ASSEMBLY, CIRCUIT DESCRIPTION

Introduction

The A19 Capacitor Assembly contains the full-wave bridge rectifiers and line filters for the +20V, and the -10V power supplies. Also located on the board is a Power-ON warning indicator for the safety of the service technician. The A19 Capacitor Assembly itself does not contain any hazardous voltages. However, if this assembly is removed before the warning indicator has extinguished, there will be hazardous voltages present on and directly beneath the A62 Main Motherboard. Allow at least one minute for the voltage to bleed off.

+20V Rectifier A

The +20V full-wave bridge rectifier consists of CR1 through CR4. C3 is a high frequency filter to attenuate diode reverse recovery transients (necessary to conform to VDE conducted line emissions standards). C5 and C6 are the main filter capacitors; R1 and R4 form a bleeder resistor.

-10V Rectifier B

The -10V full-wave bridge rectifier includes CR5 through CR8; these are schottky barrier power rectifiers and are used here to increase the efficiency of the low voltage power supplies. C4 is a high frequency filter for diode recovery transients. C7, C8, and C9 are the line filter capacitors and R2 is a bleeder resistor.

Power-on Safety Indicator C

The Power-ON LED (DS1) should be ON whenever the 8340A is connected to live AC mains. Since the 8340A has no ON/OFF line power switch, if the power cord is connected, the unregulated supplies are active. DS1 indicates that the unregulated supply filter capacitors still store enough energy to present a potential safety hazard.

A19 CAPACITOR ASSEMBLY, TROUBLESHOOTING

Red LED DS1 is primarily a safety indicator. It should warn the service technician that potentially hazardous voltages are present on the motherboard beneath the A19 Capacitor Assembly (the board itself presents no shock hazard, but can supply high current). Wait for the red light to go out before removing the A19 Capacitor Assembly to place it on a PC extender card. This extender is designed assuming the instrument is on it's left side (ON/STANDBY switch down, output connector up) and the A19

Capacitor Assembly is resting on the side rail.

If the instrument blows line fuses (and the trouble has been traced to the A19 Capacitor Assembly and not one of it's loads), the first step would be to remove aluminum electrolytic capacitors C5 through C9. If the problem dissappears, one of these capacitors is shorted; use a process of elimination to discover which capacitor is defective. If the problem persists, try to isolate the cause to one of the two power circuits by removing one of the T1 power transformer leads to the +20V winding (red leads) from the A62 Main Motherboard. It will be necessary to remove the A19 Capacitor Assembly in order to access the screws connecting the +20V leads to the A62 Main Motherboard (be careful to isolate the exposed wire from all other circuits on the motherboard). If the problem persists, C2, C4, CR5 through CR8, or R2 are shorted and must be replaced.

With the instrument in standby and the power line at a nominal level (120V in the 120V line option), you should expect +35VDC on TP1 (or directly across C5 or C6) and +18VDC directly across C7, C8, or C9. If DS1 is extinguished, but the -10V UNREG voltage level appears correct, check DS1 and R3. If the voltage level is incorrect and you have verified that the correct line voltage option has been selected, check the corresponding rectifiers for an open. If this is not the problem, the transformer should be checked.

A35 RECTIFIER ASSEMBLY, CIRCUIT DESCRIPTION

Introduction

The A35 Rectifier Assembly consists of the -40V rectifier, the input line overvoltage protection circuitry, the +5V rectifier and the +22V regulator.

-40V Rectifier A

The -40V rectifier consists of CR1 through CR4 with the high frequency filter consisting of C1 and C5.

Overvoltage Protection B

The overvoltage protection circuitry is a simple crowbar circuit that is fired in the event that a low line voltage is selected by the line module and the instrument is mistakenly plugged into a high voltage outlet. As the voltage across VR1 rises to 82.5V where it starts to conduct, it will supply gate current to crowbar SCR Q1, which will conduct and short the 40V transformer winding during each positive half-cycle of the AC line. This should blow the main fuse in the line module.

+5V Rectifier C

The +5V rectifier is arranged in a full-wave, center-tapped configuration for efficiency (i.e., only one rectifier in series with the load at any time, as opposed to two for a bridge configuration). Power rectifier U1 is a single-chip dual schottky barrier rectifier in a TO-3 package. C2 and C3 are the high frequency filters to decrease conducted line emissions; and C7 decreases the high frequency currents on the +5V UNREG line.

P/O A62 MAIN MOTHERBOARD

The A62 Main Motherboard distributes all secondary AC and unregulated DC power to those PC boards requiring these voltages. The MAINS-ON indicator (consisting of DS1, R1, and CR1) is active whenever the instrument is plugged into the AC mains. It's function is to warn the service technician that hazardous voltages are present on the Motherboard in the power supply area. (The same circuit is used to generate the 60 Hz "LINE TRIGGER" signal for the internal sweep circuitry). DS1 is the least reliable component in this circuit and if it fails, it will usually short. Considering it's placement, a failure of DS1 should not cause failure of the LINE TRIGGER function.

The power supply main heat sink is also located on the A62 Main Motherboard. It is the primary cooling system for the +20, +12,

+5.2, -10, and -40 Volt power supplies.

NOTE

The thermal connection between the pass transistors and the main heat sink is the dominant factor in their long term reliability. Be sure to properly apply thermal compound when installing or replacing these parts.

+22V Regulator D

The +22V regulator consists of U2 (a three terminal adjustable regulator), the adjustment circuitry (R1, R2, and R3), and ripple rejection capacitors C8 and C10. CR6 prevents C10 from discharging into U2 if the +22V line is shorted. CR7 prevents C8 and C10 from discharging into U2 if the input to U2 is shorted or when line power is removed. CR5 protects the +22V loads from damage due to reverse polarity power supply voltages in the event of some instrument fault. Should a direct short between the +22V and -10V power supplies occur, the -10V supply will easily overpower the +22V standby supply.

NOTE

This supply is continuously active as long as the instrument is attached to a live AC power line.

+22V Crowbar/Supply-On Indicator E

In the event of an overvoltage condition on the +22V regulated output, VR2 will conduct, delivering gate current to crowbar SCR Q2. With gate current applied, Q2 latches ON and shorts the +22V output to ground, protecting the instrument +22V loads from damage due to the overvoltage condition. C9 filters transients to prevent premature firing of Q2. DS1, R4 and VR3 comprise the Power-On indicator. DS1 will begin to light when the regulator supply voltage reaches +17V.

A35 RECTIFIER ASSEMBLY, TROUBLESHOOTING

Since the A35 Rectifier Assembly contains three separate and isolated power circuits, each circuit can be considered separately.

The -40V rectifier is straightforward, and troubleshooting follows the same logic as pointed out in troubleshooting the A19 Capacitor Assembly. When a crowbar SCR fails, it will usually

short. If the instrument blows line fuses and the problem is traced to the A35 Rectifier Assembly, check Q1 for a short (this could also be due to a shorted VR1). If the overvoltage protection circuit does not work, it is probably due to and open VR1.

The +5V rectifier has only two diodes; if this unregulated supply shows a problem, check the diodes for open or shorted condition failures.

The +22V regulator source is the +20V UNREG line; the A19 Capacitor Assembly must therefore be present to test this regulator. If the voltage at TP1 (+22V nominal) is at 0V, then either regulator U2 or fuse F1, is open. If TP1 is at approximately .8V to 1.0V, then the supply is in crowbar and Q2 is latched ON. U2 may have shorted, an open has occurred in the path to the U2 adjustment terminal, or Q2 or VR2 may be shorted. It is possible that all that is required is to readjust R3 counter-clockwise to decrease the output voltage, cycle line power to turn Q2 off, and recheck TP1.

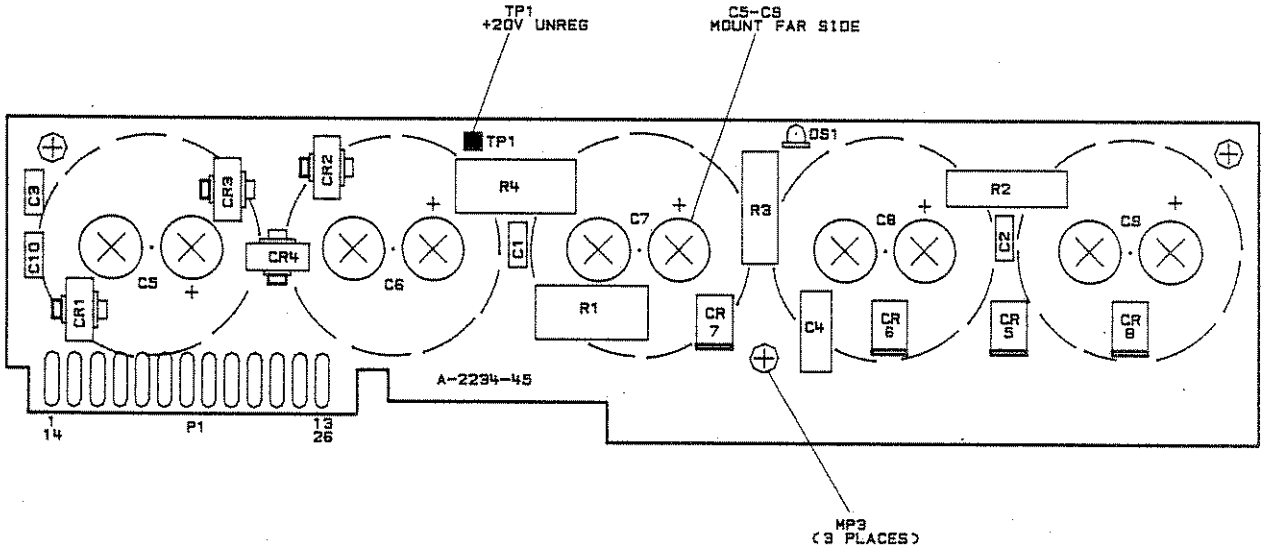


Figure 8-696. A19 Capacitor Assembly, Component Location Diagram

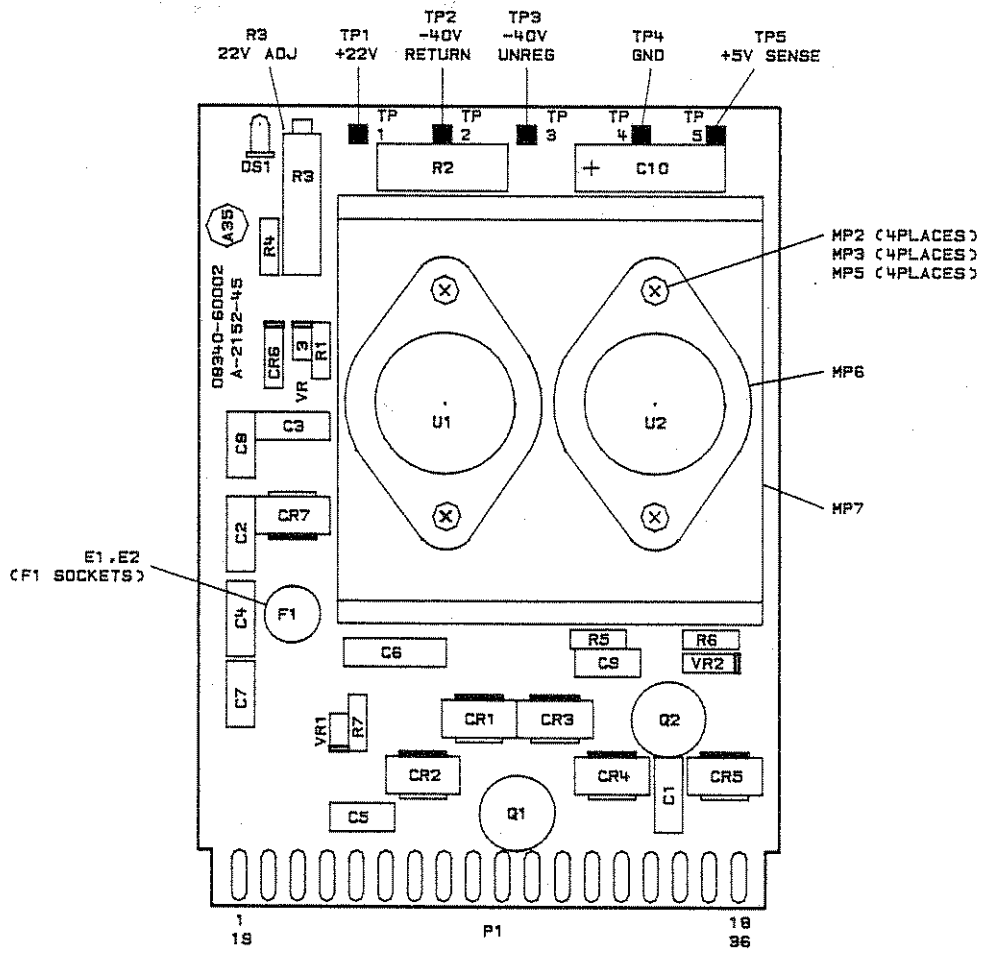
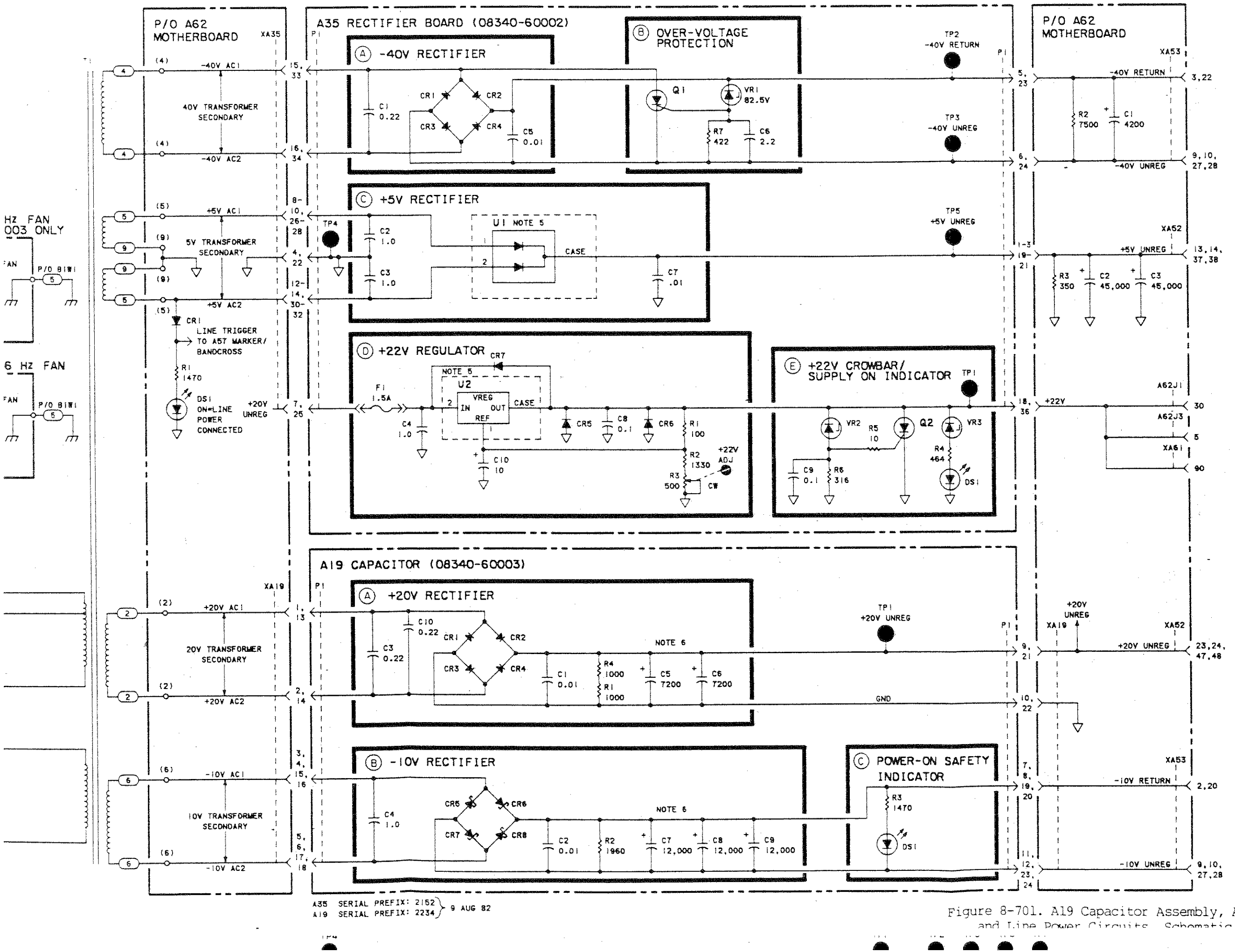


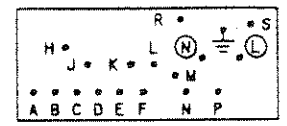
Figure 8-697. A35 Rectifier,
Component Location Diagram

P/O A6 KEYBOARD INTERFACE
+22V
R12 4640
R4 4640
P/O J4
3
P/O FRONT PANEL CHASSIS
P/O P1
P/O W50
2
3
P/O P1
POWER
ON STANDBY
NC
3
P/O W50
P/O P1
P/O W50
P/O J4
2
P/O J4
P/O P7
20
P/O A62W1
20
P/O A62 MOTHERBOARD
P/O J1
XA52
LSBY
45
CR2
K1 FAN RELAY
XA35
2
+22V
18,36
STANDBY
12
NC
J30
P1
14
ON
10
1
STANDBY
9
NC
NC
2
P2
5
ON
7
3
NOTE 4
P/O REAR PANEL
NOTE 7
C1
0.39
P/O B1W1
B1 400 Hz FAN
OPTION 003 ONLY
9
5
6
FAN
P/O B1W1
5
B1 48-66 Hz FAN
P/O B1W1
0
0
FAN
P/O B1W1
5
P/O A62
MOTHERBOARD
(4)
4
-40V AC
40V TRANSF
SECONDAR
(4)
4
-40V AC
(5)
5
+5V AC
(9)
9
5V TRANSFO
SECONDAR
9
(9)
9
(5)
5
+5V AC
(5)
CR1
LINE TRI
TO A57 M
BANDCROS
R1
1470
DS1
ON=LINE
POWER
CONNECTE
FL1 POWER LINE MODULE/LOW PASS FILTER
NOTE 3
FL1W1
0
4
LINE VOLTAGE SELECTOR PC BOARD
120/240
100/220
220/240
100/120
100/120
220/240
B
C
A
E
D
F
0
3
04
05
02
5.0A FOR 100VAC
4.0A FOR 120VAC
3.0A FOR 220VAC
2.0A FOR 240VAC
F1
LINE CORD
LINE VOLTAGE 100, 120 220, OR 240VAC +5%-10% 50-60Hz
LINE
GND
NEUTRAL
L
N
C1
0.1
918
98
54
FL1W1
SAFETY GND
(2)
2
+20V AC
20V TRANSF
SECONDA
(2)
2
+20V AC
(6)
6
-10V AC
10V TRANSF
SECONDA
(6)
6
-10V AC

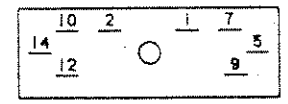


NOTES:

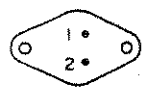
1. REFER TO FIGURE 8-X FOR DETAILED SCHEMATIC DIAGRAM SYMBOLOGY NOTES.
2. RESISTANCE VALUES SHOWN ARE IN OHMS, CAPACITANCE IN MICROFARADS, AND INDUCTANCE IN MICROHENRIES UNLESS OTHERWISE NOTED.
3. LINE MODULE PC BOARD DIAGRAM AS SEEN FROM ASSEMBLY CONNECTION SIDE:



4. BOTTOM VIEW OF A62K1:



5. BOTTOM VIEW OF A35U1,U2:



6. CAPACITORS A19C5-9 ARE LARGE ELECTROLYTICS MOUNTED TO THE A19 ASSEMBLY BY SCREWS.
7. C1 IS MOUNTED TO THE REAR PANEL ASSEMBLY IN OPTION 003 (400 Hz LINE) INSTRUMENTS ONLY.

A35 SERIAL PREFIX: 2152
A19 SERIAL PREFIX: 2234
} 9 AUG 82

Figure 8-701. A19 Capacitor Assembly, A35 Rectifier, and Line Power Circuits, Schematic Diagram

A52 POSITIVE REGULATOR CIRCUIT DESCRIPTION

Introduction

The A52 Positive Regulator contains circuitry for the +20V linear reference supply, the +12V digital supply, the +5.2V digital (and microcircuit) supply, voltage accuracy sensing circuitry for these supplies, and ON/STANDBY and SHUTDOWN functions. The +20V linear reference supply is a self-starting regulator having a precision reference to accurately set the output potential. With the exception of the independent +22V standby supply (described in the A35 theory of operation), all supplies are slaved to the +20V output. The +12V, +5.2V, -10V and -40V supplies are directly slaved while the -5.2V and -15V supplies are indirectly slaved (refer to Figure 8-682A, 8340A Power Supply Logic Block Diagram).

These supplies fall into two basic categories; critical supplies (+20V, +5.2V, -10V, -40V) with a specified periodic and random deviation (PARD) less than 100 microvolts peak (used for low-noise analog or microcircuit power), and non-critical supplies (+12V, -5.2V, -15V) with a specified PARD less than 5mV peak (used for digital and non-critical analog power).

+10V/+4.9V REFERENCE A

Zener regulator VR5 creates a stable +10V reference (+10VR) for use in the +20V Regulator (Block B), Standby/Overtemperature Shutdown (Block E), and voltage sense circuitry on the A52 Positive Regulator Assembly. VR5 bias is supplied through R26 by +20V UNREG. The accuracy and stability of VR5 is not critical; however, a large error in the voltage across VR5 can cause problems with the power Up/Down circuitry. If +10VR is incorrect, check for excessive supply loading. Trouble is indicated if the value of +10V REF changes significantly as the LINE switch is cycled. The +4.9V reference (+4.9VR) isgenerated by divider network R39 and R40. This signal is used as a reference for the comparators in the Standby/Overtemp Shutdown (Block E) and Voltage Sense (Block L) circuits on the A52 Positive Regulator Assembly.

+20V Regulator B

The +20V regulator is the master regulator for the 8340A power supply system. Except for the +22V standby supply (which is ON continuously), all instrument supplies are either powered from the +20V regulator directly (eg. +12V regulator), or use it as a reference (see FIGURE 8-682A).

Q12, Q13, and Q14 comprise the startup current source for the +20V regulator. Q12 and R14, driven from the Internal +10V

Reference (Block A) form a 6mA (nominal) current sink. C19 damps out Q12 oscillations due to excessive line length. Q13 and Q14 are connected as a Wilson current mirror with local feedback (R6 and R7) to ensure current sharing. Output current from the collector of Q14 is 6mA.

In standby, the output of U4D pin 13 (Standby/Overtemp Shutdown) is LOW, and current from Q14 is shorted to ground. When the instrument is ON, both U4D pin 13 and U4C pin 14 are open (they have open collector outputs) and current from Q14 is delivered to the base of chassis mounted darlington pass transistor Q3, acting as an emitter follower. This causes the +20V output to begin increasing.

When +20V output exceeds +10V, precision +10.00V reference U2 goes into regulation, and U1 begins to function. TP3, aside from allowing a check of U2, provides a very accurate +10.00V reference for instrument troubleshooting.

The DC feedback loop (error correction circuit) receives the +20V output through voltage divider R13 and R15 and compares it to the output of U2 by U1. The error voltage generated on the output of U1 (pin 6) is fed through CR5, R11, R8 and CR4 to the base of emitter follower pass transistor A62Q3, completing the loop. Due to the placement of CR5, U1 cannot source current to A62Q3. U1 therefore, robs base current as +20V out exceeds 20 Volts, acting as negative feedback to regulate the output voltage.

R16 and C5 form a noise filter to clean up broadband noise on integrated reference voltage source U2. They also slow down the startup transient, acting as a soft-start circuit. C4 (in conjunction with R13), C3, R12 and C2, R10 and C1, R18 and C6, are loop frequency compensation components.

R1 and R2 form the current sense resistor for the foldback current limit circuit consisting of R8, CR4, R9, and Q8. As the current from A62Q3 (Darlington pass transistors) exceeds 2.4 Amps, the voltage at the emitter of Q8 decreases sufficiently to turn Q8 on. This allows current to flow through Q8, robbing base current from A62Q3, and thus reduces the current from A62Q3. R8, R9, and CR4 sets the voltage at which Q8 turns on.

Foldback current limit is used on all critical supplies for several reasons. First, a high current supply (such as the +5.2V supply capable of delivering 10 Amps) is easily capable of damaging a PC board if an ohmic short develops on the end of a long run of PC trace. 10 Amps through 20 mil PC traces will burn them right off the board. Foldback current limit reduces this output current capability of the supply as it's output voltage drops (as in driving a dead short). A second and equally

important consideration is power dissipation in the pass transistor for this critical supply. The purpose of the foldback circuit is to have power dissipation less with the supply shorted, than with the supply in normal operation. Table 8-703A lists the maximum output current capability of each supply, and short circuit output current in foldback.

Table 8-703A. Power Supply Output Current Capability

SUPPLY	MAXIMUM OUT	SHORT CIRCUIT CURRENT
+20	2.4A	< .5 A
+12	1.8A	NO FOLDBACK (>2A)
+5	10 A	< 3 A
-5	1.8A	NO FOLDBACK (>2A)
-10	6.0A	< 3 A
-15	1.8A	NO FOLDBACK (>2A)
-40	1.7A	< .5 A

CR10 protects instrument loads from reverse polarity power in the event of a short between the +20V output and some negative polarity power supply.

+20V Crowbar/Power On Indicator C

VR1 and R20 monitor the +20V regulator output. When this voltage exceeds approximately 23V, the drop across R20 is large enough to gate crowbar SCR Q1 ON and short the supply output to ground. This circuit is useful for protecting instrument loads in many fault conditions. If the +20V crowbar circuit did not exist and pass transistor A62Q3 should short, for example, the +20V output voltage would increase to the level of +20V UNREG (approximately 35V); this would easily destroy most circuitry tied to the +20V supply bus.

Yellow LED DS2, mounted close to TP4, and current limit resistor R21 give a visual indication of the status of the +20V power supply. By observing this indicator along with the indicators for the other supplies, the status of all the instrument power supplies can be easily determined.

Reference Oscillator Supply D

When HSTD is asserted HIGH by the microprocessor, Q4 conducts, turning saturated series switch Q5 ON. This brings the +20V Reference Oscillator Supply output up to power ON the A51 10 MHz Reference Oscillator.

Standby/Overtemp Shutdown E

In STANDBY mode LSBY is pulled LOW by the front panel ON/STANDBY switch. This drives U4D pin 13 (the open collector output of quad comparator U4, Standby/Overtemp Shutdown Block E) LOW which in turn, through CR7, pulls the base of chassis mounted +20V pass transistor Q3 to ground. The +20V supply is shut down, along with all other supplies that are slaved to it. Also notice that CR13 pulls the CLK input to D-type flip flop U5 LOW (U5 is a positive edge triggered CMOS D-type flip flop).

When the ON/STANDBY switch is flipped to the ON position, LSBY rises to +22V, back biasing CR6. The voltage across C9 rises exponentially toward 5V. When it passes 4.9V, U4D pin 13 goes HIGH (open) and the base of chassis mounted Q3 is released. The +20V supply starts itself. CR13 now causes the CLK input to U5 to go HIGH (but not to exceed the 10V Vcc). This transition clocks a zero into the flip flop (due to the D input, which is tied low), resetting any overtemperature condition that may have occured. During initial power-up, C10 and R53 reset U5 to ensure that the instrument is always in operational status (with overtemp flag cleared) when initially energized.

The main heat sink temperature sensor is a normally open bi-metallic switch that closes when the heat sink reaches 100 degrees C. The sensor is tied from LHSOT to ground, so that a switch closure pulls LHSOT LOW and forces U4B pin 1 HIGH, which in turn sets flip flop U5. Q output goes HIGH, forcing U4A pin 2 HIGH and turning ON red overtemp indicator LED DS4. Q NOT output goes LOW forcing U4C pin 14 LOW which in turn pulls the base of chassis mounted Q3 to ground, shutting the instrument power supplies down. U5 has now latched this overtemp condition, and subsequent removal of LHSOT (as when the heat sink cools back down) does not cause the instrument to restart. The only way to clear this overtemp condition is to turn the ON/STANDBY switch to STANDBY, and then back to ON.

This overtemp protocol was specifically chosen for several reasons. First of all, a fault condition that allows the main heat sink to reach 100 degrees C indicates that something is drastically wrong (e.g. the fan has stopped, etc.). The possibility of a fire is not out of the question. Therefore, it was decided that once the overtemp condition is detected and the instrument has shut down, it should take a specific operator intervention before the instrument will restart. This should call attention to a possibly hazardous situation. Because the over temperature detector latches when overtemp is detected, the 8340A will not cycle ON and OFF repetedly if there is a condition that causes overheating. This eliminates cycling at excessively high temperatures which could affect the reliability of the

instrument.

Grounds and Commons F

Ground distribution is very critical on this board to achieve the PARD specification for the +20V and +5.2V regulators. Right at the edge connector finger power ground (plain ground), sense ground (ground 1), and +20V ground (ground 2) are separated. This is to isolate power ground currents from sensitive circuitry in the regulators.

+5.2V Regulator G

+20V provides the reference voltage, and powers the loop error correction amplifier U3. R67 and R68 drop +20 Volts to 4.01 Volts. C14 is a noise filter, and also acts as a soft-start element (it slows down the power supply turn-on transient). +5.2V out is sensed remotely on the A62 Main Motherboard at the main 5V power distribution point. +5.2V SENSE(+) comes back onto the board, into voltage divider R65, R66, and is compared to the generated 4V reference by error amp U3. The error voltage is fed to emitter follower Q7, then to darlington driver Q10, and then to the chassis mounted pass transistor, Q4. The +5.2V SENSE(-) comes from the central ground distribution point (STAR ground) on the A62 Main Motherboard to provide ground reference.

Loop frequency compensation uses the feedforward technique, with C13 (in parallel with R65) and C16, R63, R64 and C12. R69 and C15 lower output impedance and provide a minimum load capacitance. Foldback current limit operates in essentially the same manner as in the +20V supply. The current sense resistor is the parallel combination of R3, R4, and R5. Foldback is accomplished with pre-bias from R61 and R62, and Q6 is the active element.

+5.2V Crowbar/Protection H

When +5.2V OUT exceeds approximately 6.2V, VR3 conducts, providing gate current for crowbar SCR Q11. It latches ON and shorts the +5.2V output to ground, protecting load circuits from the overvoltage condition. CR12 protects against reverse polarity applied to the load due to some instrument fault, and yellow LED, DS1 provides a visual indication of the operational status of the supply.

Microprocessor Protection I

VR4 senses the -5.2V supply, and anytime its level is more positive than -4.5V, Q3 is turned ON. This shorts the adjustment terminal of A62U1 (the +12V regulator in +12V Regulator Block E) to ground, pulling +12V output down to +1.3V. This circuit

prevents the microprocessor from being damaged by excessive power dissipation. For this reason, after work has been done on either the +12V or -5.2V Regulators, it is critical that the operation of this circuit be checked prior to turning the instrument ON with the microprocessor board in the instrument.

+12V Regulator J

A62U1 is an adjustable three-terminal regulator. Output voltage is adjusted by the selection of the feedback resistors R29, R30 and A62R14. R30 and A62R14 are fixed values whle R29 is a factory select. Through proper selection of R29, compensation for variations in regulator characteristics is obtained. The nominal value of R29 is 4.22K and is appropriate for most of the regulators. However, it may be necessary to substitute an alternate value. Increasing R29 increases the +12V output. A62R14 is mounted on the A62 Main Motherboard in parallel to R29 to ensure that the regulator has a ground reference path before it's feedback is connected (as in inserting the A52 Positive Regulator Assembly with the power ON).

Input capacitor A62C7 is required for stability of the regulator. A62C6 is a noise filter and increases the ripple rejection of the regulator and lowers it's output impedance. A26CR3 is required to protect the regulator from damage due to charge stored on C6 in the event of a short from the +12V output to ground. CR11 protects the +12V power supply's loads from reverse polarity power inn the event of a short between +12V and some negatine power supply. R31 and C17 reduce the output impedance of the supply, and provide a minimum capacitive load to guarantee stability regardless of load configuration.

+12V Crowbar/Power On Indicator K

When +12V OUT exceeds approximately 13.5 Volts, VR2 conducts, providing gate current for crowbar SCR Q2, latching it ON and shorting the supply output to ground. This protects load circuits from damage due to the overvoltage condition. Yellow LED, DS3 gives a visual indication of the status of the +12V power supply. It will begin to light when the output of A62U1 is approximately +7.6V.

Voltage Sense L

U6A, U6D, and U6B sense the level of the +5.2V, +12V and +20V power supplies. When one of these supplies goes out of regulation it's comparator output goes LOW, shorting delay capacitor C8 to ground. This forces HPUP LOW and asserts LIPS LOW. CR9, CR14 and CR15 are provided to easily isolate which supply caused the low voltage indication.

The cathode of CR8, High Negative Up (HNUP) goes to the A53 Negative Regulator and A56 -15V Supply boards. This line is pulled LOW in the event any of these supplies go out of regulation.

When all supplies come into regulation, C8 is released and it's voltage increases as it is charged by R49. After some 300mS it's level passes VREF at 4.9 volts and U6C pin 14 goes LOW. This asserts HPUP HIGH via Q16 and sets LIPS HIGH via Q15. These signals are used by the processor (and several other circuits) to control instrument activity and to ensure proper initialization.

A52 POSITIVE REGULATOR, TROUBLESHOOTING

If all supplies appear to be down, the first priority is to troubleshoot the +20V Regulator (Block B). If this supply is down the rest of the instrument will be shut down. Look at +20V OUT. If it is in crowbar (approxximately 0.8V to 1.0V), checck error amp U1 and follow the feedback path to see where it is broken; also check the crowbar circuit itself. If +20V OUT is at ground, (e.g. less than .3V), the problem is probably not that the supply has been crowbarred. The startup current source should be checked next. Find out if Q14 collector is sourcing any current, and where it is going. Check for internal +10V reference. (measure across VR5 in the +10V/+4.9V Reference, Block A) to see that this supply is up. Also check VREF at the junction of R39 and R40 in the +10V/+4.9V Reference (Block A), and at U4 in the Standby/Overtemp Shutdown (Block E).

Check for a shorted Q8 (current limit device in +20V Regulator, Block B). If the collector of Q14 is held LOW by U4C pin 14, the level will be lower than if U4D pin 13 is holding it LOW (this tells you whether the instrument thinks it's in STANDBY or OVERTEMP shutdown mode). If it is shutdown by U4D pin 13, something is wrong with it or R58, R59, C9, or LSBY. If it's shutdown by U4C pin 14, trace the signal back to find where the problem lies.

If the value of +20V OUT is incorrect, check the +10.00V precision reference (U2), and the values of divider resistors R13, R15, and the leakage currents of tantalum capacitors C4 and C5. If the supply has excessive temperature drift in VOUT, again check leakage currents in C4 and C5 ($I1 = K * C * E$ where C is capacitance, E is rated working voltage, and K is .01 at 25 degrees C and .2 at 85 degrees C. For C4, $I1 \leq 3.3$ microamps at 25 degrees C and 66 microamps at 85 degrees C. For C5, $I1 \leq 3$ microamps at 25 degrees C and 60 microamps at 85 degrees C). If leakage is excessive, one or both parts must be replaced. Leakage in C4 and C5 is the primary limit on the temperature stability of

+20V OUT.

If the +12V regulator is down, remember that this supply comes up only when the +5.2V and -5.2V supplies are both operating properly. If the A53 Negative Regulator board is not installed, nothing will get the +12V supply up. The best way to tell which circuit caused the shutdown is to measure the base of Q3 in the Microprocessor Protection circuit (Block I). If it is turned ON (.6V or greater), then VR4 is open or the -5.2V supply is down. If it is OFF, then U6B pin 1 in Voltage Sense (Block L) has caused the problem. Trace backwards to find out why.

If the +20V switched supply doesn't come up (or won't shut down), check driver Q4 and pass element Q5 in Reference Oscillator Supply (Block D). Ensure that HSTD is getting to the board properly.

The +5.2V supply exhibits many problems in common with the +20V supply. If VOUT is slightly off value or excessively temperature sensitive, look at leakage current in C14 (<3.3 microamps at 25 degrees C and 66 microamps at 85 degrees C), and the values of R65 thru R68. If the supply is down, check the power supply to U3 in +5.2V Regulator (Block G). Check it's operation, look at Q7 and Q10, and check for shorted Q6. If the supply is in crowbar, follow the feedback loop around and look for opens, or check Q11 and VR3 for shorts.

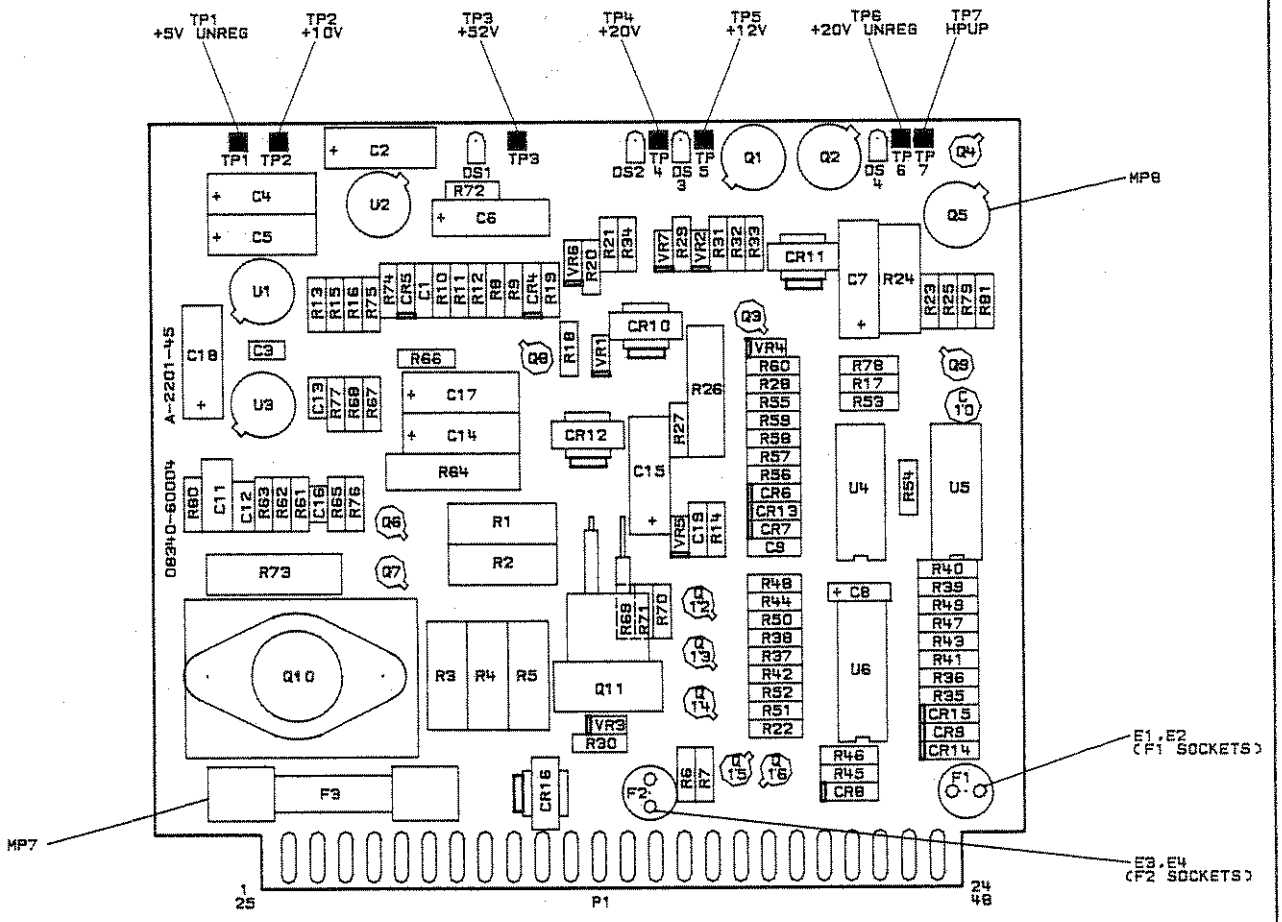
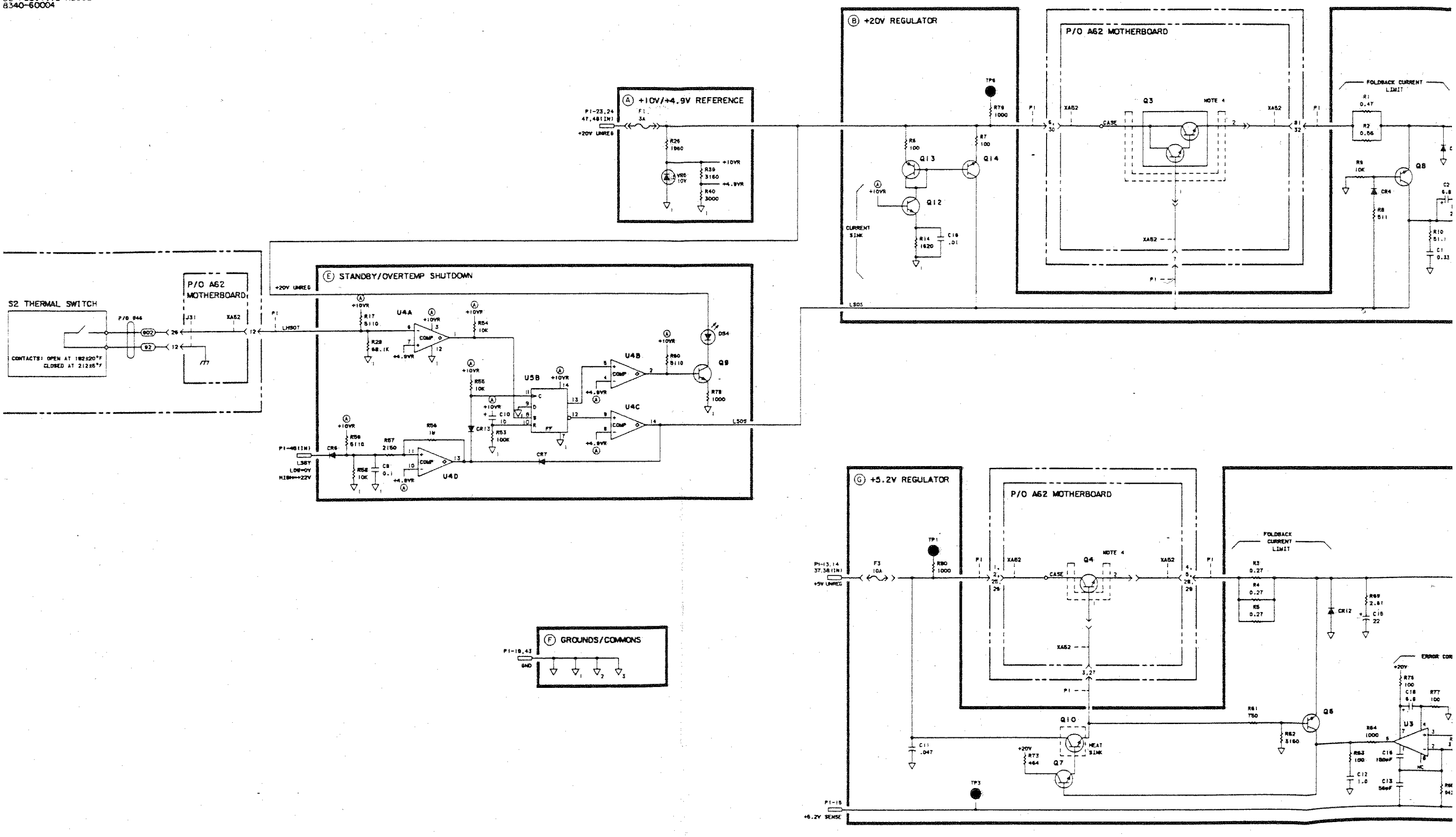


Figure 8-705. A52 Positive Regulator, Component Location Diagram

52 POSITIVE REGULATOR
8340-60004



7 SERIAL PREFIX: 2201-46 14 SEPT 82

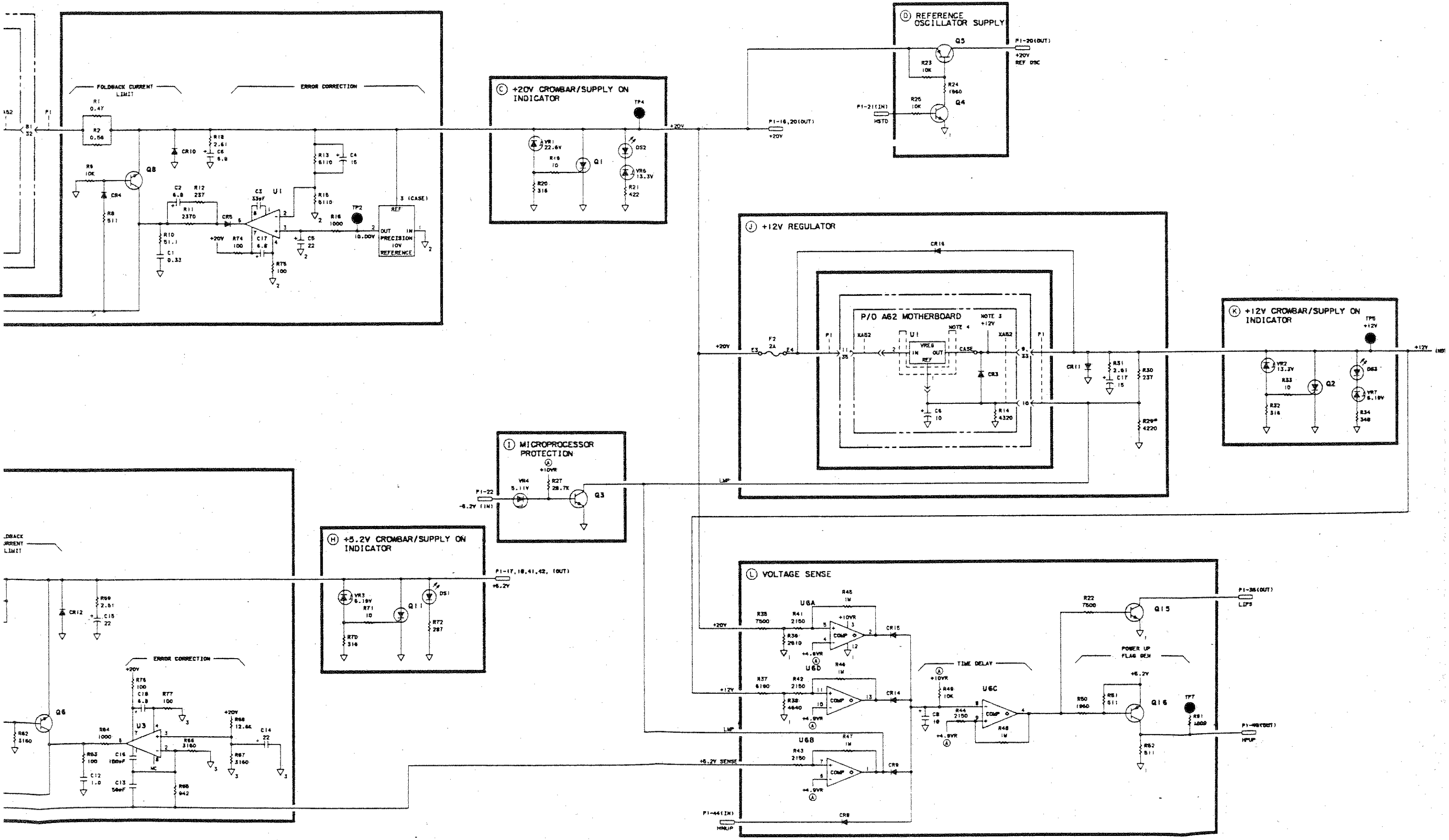


Figure 8-707. A52 Positive Re

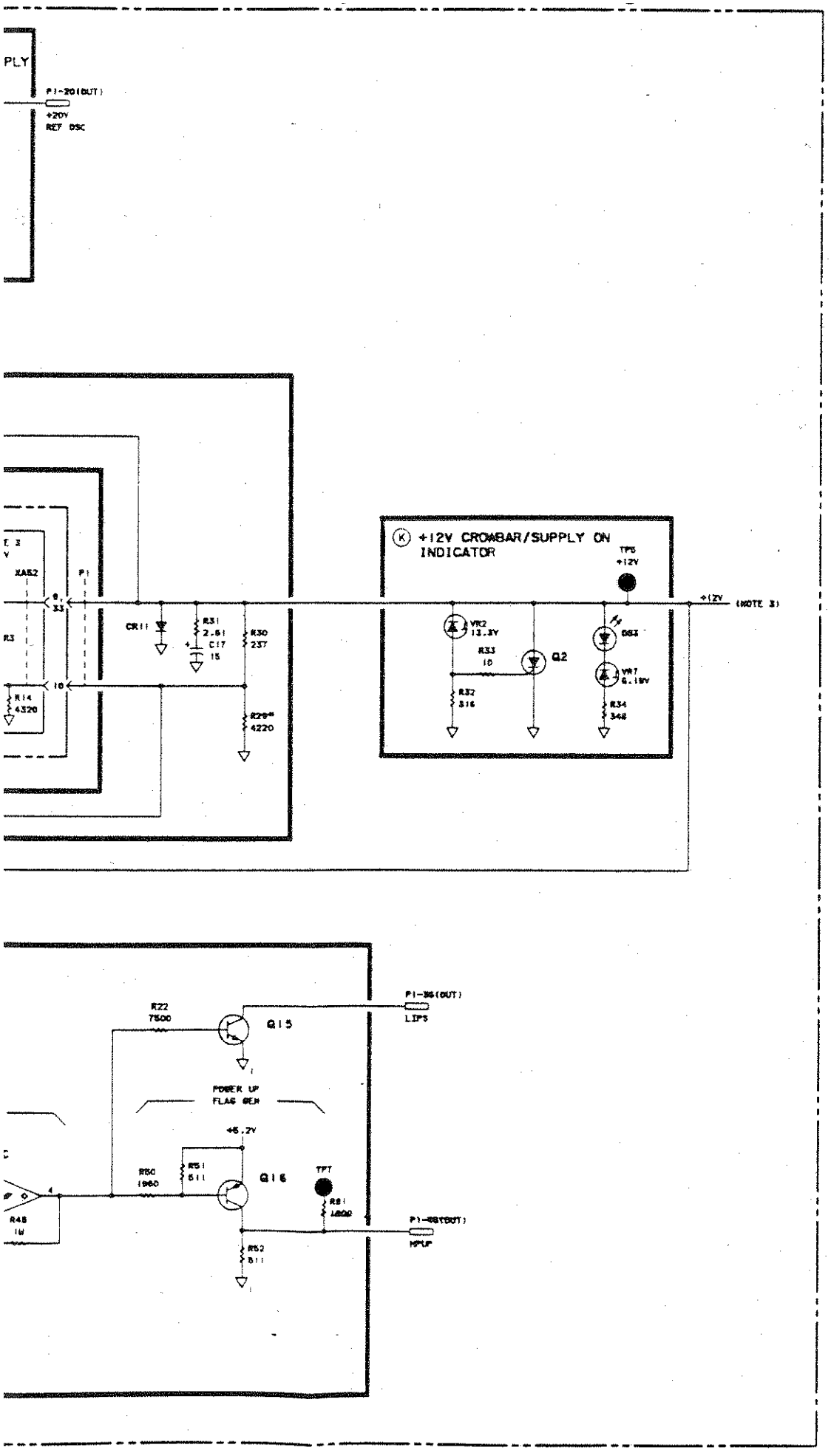


Figure 8-707. A52 Positive Regulator, Schematic Diagram

A53 NEGATIVE REGULATOR
08340-60005

P/O A62 MOTHERBOARD

-10V RETURN
Q1
CASE
NOTE 4
XA53
7,8
25,
26
P1
4
2,20
-10V UNREG
9,10
27,
28

(A) -10V REGULATOR
FOLDBACK CURRENT LIMIT
ERROR CORRECTION
R1 0.47
R2 0.47
R3 0.47
CR4
R4 825
Q4
CR5
R5 6810
R7 1000
C1 33pF
U4
+20V
+20V
R8 3160
R9 3160
C5 22
C3 1.0
R6 100
CR6
C4 .047
R10 3160
TP1
R52 1000
F3 6A
CR7
C6 15
R11 2610

(B) -10V CROWBAR/SUPPLY ON INDICATOR
TP6 -10V
-10V
R12 316
R13 10
Q6
DS3
VR7 5.11V
VR1 11.0V
R14 237

(C) -5.2V REGULATOR
CR16
R15 2.2
R18 2.2
F1 2A
E1
E2
U1 NOTE 3
VREG
IN
OUT
CASE
REF
C7 1.0
HEAT SINK
CR15
CR8
C8 1.0
R17 100
C14 10
R16 316

(E) -40V REGULATOR
FOLDBACK CURRENT LIMIT
ERROR CORRECTION
-40V RETURN
Q2
CASE
NOTE 4
XA53
1,19
P1
21
3,22
-40V UNREG
6,24
-40V SENSE
23
R22 0.68
R23 1000
Q2
Q3
TP2
CR10
R53 1000
CR9
R24 28.7K
C10 1.0
R25 100
VR4 10.0V
R30 3160
C2 33
U3
+20V
+20V
R27 3160
R28 3160
C12 22
CR11
R29 12.6K
C11 .042
F2 1.5A
E3
E4
TP4 -40V
CR12
C13 10.0
R31 2610

(F) -40V CROWBAR/SUPPLY ON INDICATOR
-40V
R32 316
R33 10
Q5
DS2
VR8 30V
VR3 44.2V
R34 750

P/O A62 MOTHERBOARD
-40V
XA53
XA56
3,18
30
P1

A56-15V SUPPLY
08340-60029

(A) -15V REGULATOR
R6 22
R1 22
TP1 IN
F1 1A
E1
E2
U1 NOTE 3
VREG
IN
OUT
CASE
REF
C1 1.0
HEAT SINK
CR3
CR2
C3 1.0
CR1
VR4 13.7V

XA56
P1
5,
20
(D) GROUNDS/COMMONS

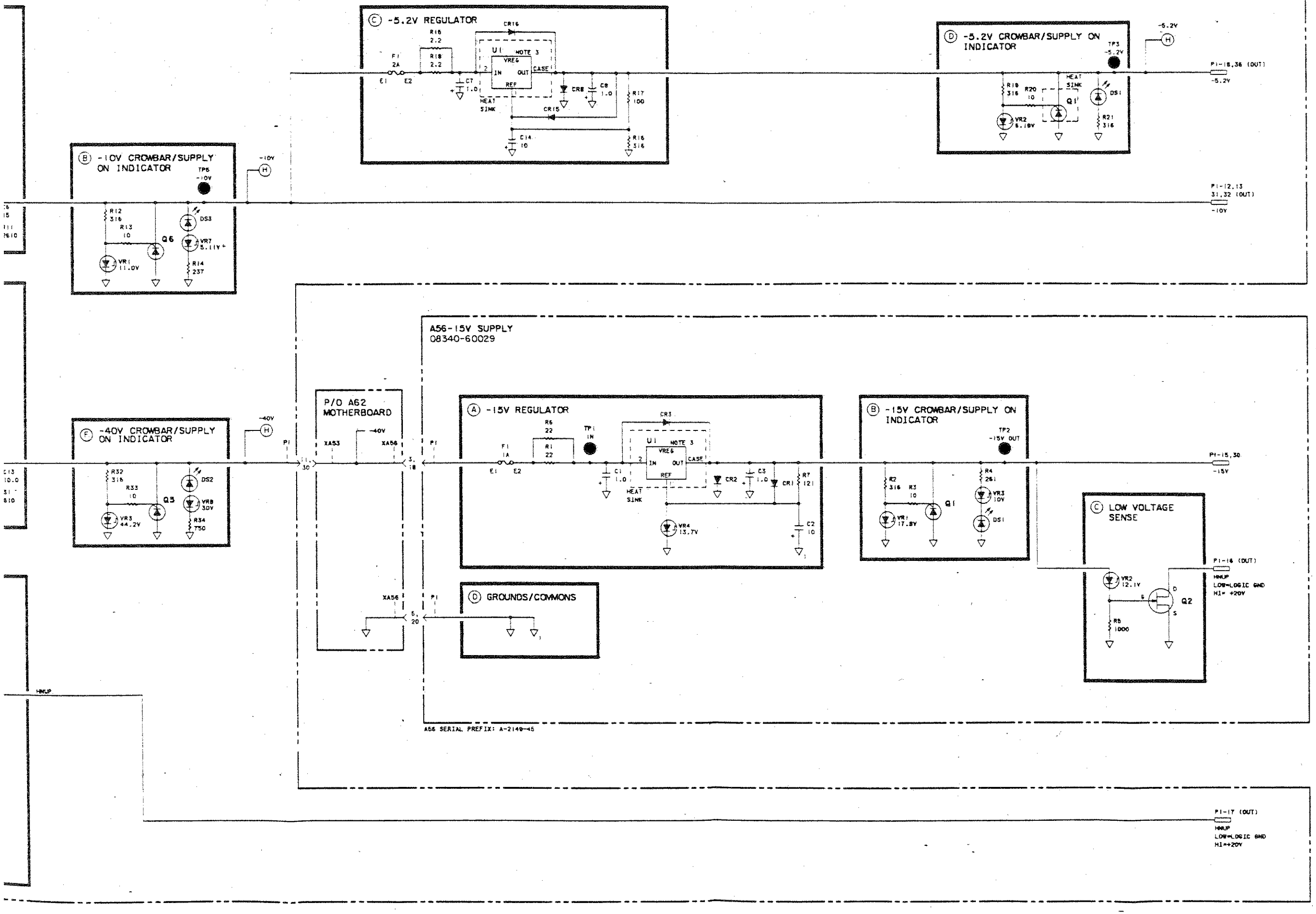
(G) -4.64V REFERENCE
-10V
R35 261
VR5 4.64V

(H) VOLTAGE SENSE
R41 10M
R40 10K
U2A
CR2
-4.64VR
-5.2V
(D)
-10V
R39 10M
R38 10K
U2B
CR1
(B)
-10V
R37 10K
R36 10K
R43 10M
R42 10K
U2C
CR3
CR14
VR6 31.6V
R51 10K
-40V
(F)
R50 4220
POWER UP FLAG GEN
-4.64VR
R45 10M
R44 10K
U2D
R46 10K
+20V
R47 10DK
CR13
+20V
R49 10K
R48 10K
Q7
TP5 HNUP
R54 1000
HNUP

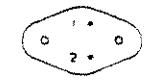
(D) GROUNDS/COMMONS
P1-14,15,18
33,34,35
GND

A53 SERIAL PREFIX: A-2153-48 & SEPT 82

A56 SERIAL PREFIX: A-2149-45



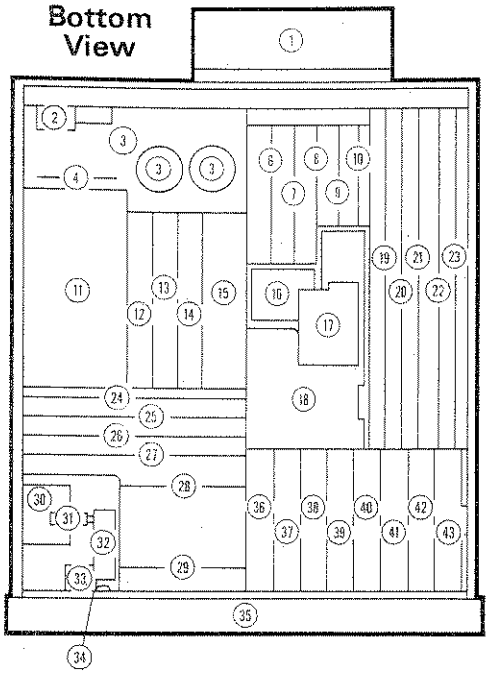
1. REFER TO FIGURE 8-X FOR DETAILED SCHEMATIC DIAGRAM NOTES.
2. RESISTANCE VALUES ARE IN OHMS, CAPACITANCE IN MICROFARADS, AND INDUCTANCE IN MICROHENRIES UNLESS OTHERWISE NOTED.
3. BOTTOM VIEW OF A53U1, A56U1, A62Q1, Q2.

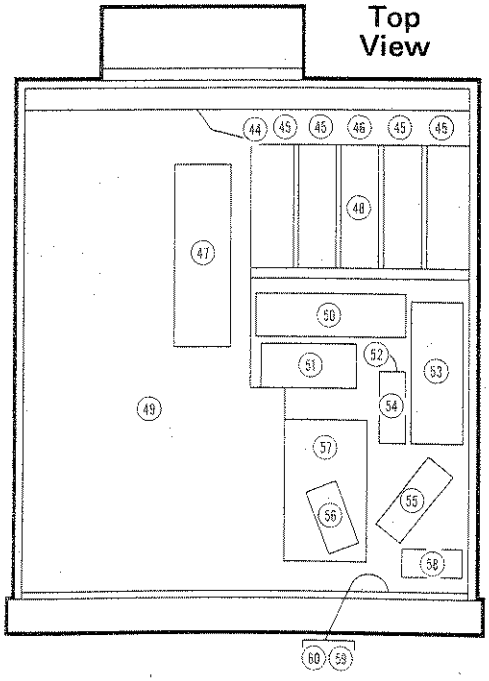


4. A62Q1, Q2 ARE MOUNTED THROUGH THE REAR PANEL HEAT SINK ASSEMBLY.

Figure 8-715. A53 Negative Regulator and A56 -15V Regulator, Schematic Diagram

REFERENCE GUIDE TO SERVICE DOCUMENTATION





Assy./Ref. Des.	Description	Location	Volume 2: Ref.-M/N Loops	Volume 2: 20/30 Loops	Volume 2: Swp. Gen.-YO Loop	Volume 2: Motherboard	Volume 2: Controller	Volume 3: Front/Rear Panel	Volume 3: RF Section	Volume 3: Power Supplies
A1	Alpha Display	35					•			
A2	Display Driver	35					•			
A3	Display Processor	35					•			
A4	Not Assigned	-								
A5	Keyboard	35					•			
A6	Keyboard Interface	35					•			
A7	Lower Keyboard	35					•			
A8	3.7 GHz Oscillator	57						•		
A9	Band 0 Pulse Modulator	56						•		
A10	Directional Coupler	32						•		
A11	Band 1-4 Detector	31						•		
A12	Band 0 Detector	34						•		
A13	SYTM (Switched YIG Tuned Multiplier)	10						•		
A14	Band 1-4 Power Amplifier	53						•		
A15	Band 0 Low Pass Filter	52						•		
A16	Band 1-4 Modulator/Splitter	1						•		
A17	Band 0 Mixer	54						•		
A18	Band 0 Power Amplifier	55						•		
A18A2	Band 0 Splitter	60						•		
A19	Capacitor Assembly	48							•	•
A20	RF Section Filter	50						•		
A21	Pulse Modulator Driver	29						•		
A22	Not Assigned	-								
A23	Not Assigned	-								
A24	Attenuator Driver/SRD Bias	28						•		
A25	ALC Detector	27						•		
A26	Linear Modulator	26						•		
A27	Level Control	25						•		
A28	SYTM Driver	24						•		
A29	Reference Phase Detector	12	•							
A30	100 MHz VCXO (Voltage Controlled Crystal Osc.)	13	•							
A31	M/N Phase Detector	4	•							
A32	M/N VCO (Voltage Controlled Osc.)	15	•							
A33	M/N Output	15	•							
A34	Reference-M/N Motherboard	5	•							
A35	Rectifier	4							•	•
A36	PLL1 VCO (Voltage Controlled Osc.)	36		•						
A37	PLL1 Divider	37		•						
A38	PLL1 IF	38		•						
A39	PLL3 Upconverter	39		•						
A40	PLL2 VCO (Voltage Controlled Osc.)	40		•						
A41	PLL2 Phase Detector	41		•						
A42	PLL2 Divider	42		•						
A43	PLL2 Discriminator	43		•						
A44	YIG Oscillator (YO)	6			•					
A45	Pre-Leveler	13			•					
A46	7 GHz Low Pass Filter	18			•					
A47	Sense Resistor Assembly (YO circuit) (STYM circuit)	47 47			•			 •		
A48	YO Loop Sampler	18			•					
A49	YO Loop Phase/Detector	18			•					
A50	YO Loop Interconnect	17			•					
A51	Reference Oscillator	16	•							
A52	Positive Resulator	8							•	
A53	Negative Regulator	7							•	
A54	YO Pretune DAC/Delay Compensation	8			•					
A55	YO Driver	9			•					
A56	-15V Regulator	10							•	
A57	Marker/Bandcross	19				•				
A58	Sweep Generator	20			•					
A59	Digital Interface	21				•				
A60	Processor	22				•				
A61	Memory	23				•				
A62	Main Motherboard	49					•			
A63	70 dB RF Attenuator	55						•		
AT1	Peripheral Mode Isolator	58						•		
B1	Fan Assembly	1								•
A62C1-3	Power Supply Filter Capacitors	3								•
FL1	AC Line Module	2								•
A62Q1-4	Power Supply Regulating Transistors	-								•
A62S1	Power Supply Thermal Switch	44								•
T1	Power Supply Transformer	11								•
A62U1	Power Supply Regulator	46								•

A53 NEGATIVE REGULATOR, CIRCUIT DESCRIPTION

The A53 assembly contains all circuitry for the -10V, -5.2V, and -40V power supplies, as well as voltage sensing circuitry to flag the A52 Positive Regulator board should one of these supplies go out of tolerance.

NOTE

The -10V and -40V supplies are critical, low-noise supplies as described in the A52 Positive Regulator circuit description section. They are limited to a PARD <100^109V peak. The -5.2V supply is primarily a digital (ECL) supply, and has a PARD specification of 5mV.

-10V Regulator A

+20 VREF (P1 pin 29) comes onto the board from the A52 Positive Regulator. It is used as a reference through voltage divider chain R8, R9, and R10, and it powers up error amp U4. C5 is the soft-start element (it slows down the -20V supply turn-on transient). CR6 protects the input stage of U5 during startup. The DC feedback loop is completed through R7, CR5, and darlington driver (chassis mounted) Q1. The topology of this regulator is somewhat unique. The pass element (chassis mounted Q1) is in the ground leg, not the Vout leg. This circuit is regulating ground, and forcing -10V to float 10 Volts away from it, rather than the more standard technique of regulating Vout. This allows the use of an NPN pass transistor used as an emitter follower rather than in the common emitter configuration, which is more sensitive to supply loading.

C1, C4, R6, and C3 are frequency compensation components. R11 and C6 provide a minimum load capacitance and lower output impedance. Foldback current limiting is used here as on the +5.2 and +20V supplies. The parallel combination of R1, R2, and R3 forms the current sense resistor. CR4 compensates for the extra Vbe in the monolithic darlington pass transistor (Chassis Mounted Q1). Q4 is the active element, and foldback is accomplished through pre-bias from R4 and R5.

-10V Crowbar/Supply On Indicator B

Should -10V OUT exceed approximately 11V, VR1 will conduct, providing gate current to crowbar SCR Q6. It will latch ON, protecting load circuits from the overvoltage condition. Yellow LED DS3 provides a visual indication of the -10V supply operational status. CR7 in -10V Regulator circuit (Block A)

protects load circuits from reverse polarity power should a short develop between the -10V OUT and some high current positive supply output.

-5.2V Regulator C

U1 is a monolithic three-terminal adjustable negative regulator. The adjustment terminal is nominally 1.25V above the output terminal, so Vout is programmed by the following relationship:

$$Vout = -1.25 [1 + R16/R17]$$

C14 increases ripple rejection for U1. CR15 provides a discharge path for C14 when Vout is shorted to ground. C8 is required by the regulator for stability, and C7 is required to reduce the apparent electrical length of the supply input leads. R15 lowers the power dissipation in U1 by reducing it's operating junction temperature. R18 and C9 provide a minimum capacitive load for the supply.

-5.2V Crowbar/Supply On Indicator D

When -5.2V OUT exceeds approximately 6.2 volts, VR2 conducts, providing gate current for crowbar SCR Q1, latching it ON and shorting -5.2V OUT to ground. Yellow LED DS1 provides a visual indication of the operational status of the supply, and CR8 is provided to protect load circuits from damage due to reverse polarity power in the event of some instrument fault.

-40V Regulator E

+20V REF provides reference (through divider R27, R28, R29) for the regulator, and powers error amplifier U3. VR4 limits the negative supply to U3 at -10V. C12 is the soft-start element, slowing down the power supply turn-on transient. CR11 protects the input stage of U3 during startup. The forward path is completed through R26, CR10, darlington driver Q3, and pass transistor (chassis mounted) Q2. CR9 protects the base-collector junction of Q3 during startup (when Ic of chassis mounted Q2 is low enough, its beta is less than 1, and the base-collector junction of Q3 can be forward biased). Then if a large current flows, Q3 will be destroyed.

Feedback is completed off the board using remote sense at the main -40V distribution point on the A62 Main Motherboard. -40V SENSE comes back onto the board to complete the loop. Ground reference (Ground 2) connects to main ground on the board at the edge finger to reduce the perturbations in the supply due to noise currents in the ground trace on the board. R31 and C13 provide a minimum load capacitance.

-40V Crowbar/Suppply On Indicator F

When -40V OUT exceeds appproximately 44.2 volts, VR3 conducts providing gate current for Q5 which latches ON, shorting the supply to ground and protecting load circuits from the overvoltage condition. Yellow LED DS2 provides a visual indication of supply operational status, and CR12 in -40V Regulator circuit (Block E) protects load circuits from damage due to reverse polarity supply power in the event of some instrument fault condition.

Voltage Sense H

VR5 in -4.64V Reference (Block G) provides a -4.64V reference to compare with each supply output. Should any supply be out of regulation (low output), the corresponding comparator output will go LOW, forcing U2D pin 13 HIGH which turns ON Q7 to pull HNUP LOW (the logic level on HNUP is: HIGH = +20V; LOW = +.2V).

U2A monitors the -10V supply, U2B monitors the -5.2V supply, and U2C monitors the -40V supply. The input common mode range of U2 includes it's negative supply (U2A pin 12, connected to -10V). However, if Vin goes more negative than U2A pin 12, the device will destroy itself. The problem is that in the event of a crowbar (or short to ground) on the -10V supply, U2 pin 12 is pulled up to ground. The -40V supply, however, is still up, and can source sufficient current to destroy U2. Clamp diode CR14 and current limit resistor R51 prevent this problem from occuring. Now U2C pin 8 follows the -10V supply at U2 pin 12 when it is shorted. Diodes CR1, CR2, and CR3 isolate the outputs of U2A, U2B and U2C. This will allow checking each supply independently for low output.

Grounds And Commons I

This block attempts to depict schematically the critical power and signal ground distribution system implemented on the board. Caution has been used in deciding which load goes where, and in isolating critical ground paths from non-critical or high current ground paths on the board.

A53 NEGATIVE REGULATOR, TROUBLESHOOTING

Operation and troubleshooting of the negative regulators are virtually the same as their positive counterparts.

If nothing is working, look at +20V REF and check the levels of op-amp power supplies (U3 and U4). Also verify that the -10V UNREG and -40V UNREG lines are operating correctly. Realize that the -5.2V Regulator (Block C) is dependent upon the -10V supply; if the -10V supply is down, so is the -5.2V supply. In this case, repair the -10V supply before troubleshooting the -5.2V supply. The same is true of the -40V and -15V supplies, with minor differences. In this case, if the -15V supply crowbars it throws the -40V supply into foldback current limit. You have to separate out which supply is forcing both supplies down (if it is the -15V supply, R1 in the -10V Regulator (Block A) should indicate a healthy current through A56U1. If the -40V supply failed, there should be almost no current into A56U1.

When a supply fails to energize, first measure its output voltage. If the voltage is in the area of -0.8 to -1.0 volt, the supply is in crowbar.

CAUTION

Do not remove the crowbar and operate the supply without it. This could cause severe damage to the instrument if the supply is faulty and the crowbar has tripped to protect the instrument.

Possible failures could involve the crowbar circuit or the supply itself. If the supply output is at ground, the pass element could be open, or in a discrete regulator the feedback loop could be open somewhere (-10V and -40V supplies). If the adjustment terminal of A56U1 is open, -5.2V OUT goes to about -9V (and hopefully the crowbar fires). In the -10 and -40V supplies, if the current limit transistor shorted, V OUT, would drop to ground (essentially).

If the supply output has incorrect voltage, or is excessively temperature sensitive, examine the feedback loop very carefully. For the discrete supplies, leakage currents of soft-start capacitors C5 and C12 have a strong effect on supply output tolerance and temperature drift. For the -5.2V supply, tolerance and drift are constrained primarily by the monolithic regulator U1.

A56 -15V SUPPLY, CIRCUIT DESCRIPTION

The A56 board contains the -15V regulator and voltage sensing circuitry to flag the A52 Positive Regulator if an out of tolerance condition in the supply occures.

-15V Regulator A

U1 is a monolithic three-terminal adjustable negative regulator. It is designed to maintain a constant -1.25V difference between the OUT terminal and the ADJ terminal. With the ADJ terminal connected to VR4, the output voltage is:

$$Vout = -(1.25 + 13.7)$$

C2 improves the ripple rejection of U1, and CR1 provides a discharge path for C2 in the event of a short from -15V OUT to ground. C3 is required to compensate for the effective line length in the input circuit due to R1 and R6. R1 and R6 will reduce the power dissipation in U1 during crowbar.

-15V Crowbar/Supply On Indicator B

When V OUT exceeds approximately 17.8 Volts, VR1 conducts, latching crowbar SCR Q1 ON and shorting -15V OUT to ground. This protects instrument load circuits from the overvoltage condition. Yellow LED DS1 gives a visual indication of the supply status, and CR2 protects against an inadvertant short between -15V OUT and some high current positive supply (it clamps -15V OUT at Approximately +0.8V, protecting load circuits from damage).

Low Voltage Sense C

When -15V OUT exceeds 12.1V (VR2) + Vp (Q2, ~2V), Q2 turns OFF and HNUP goes HIGH. HNUP is used on the A52 Positive Regulator board to determine that the -15V output is within tolerance.

A56 -15V SUPPLY, TROUBLESHOOTING

If the -15V supply appears to be down, measure its output voltage. If it is at ground, regulator U1 or fuse F1 has opened. If it is between -0.8 and -1.0 Volts, the crowbar is ON. (This could be due to a failure in the crowbar with Q1 or VR1 shorted, or the pass element U1). Do not simply remove Q1 to see if that was the problem. If U1 has shorted, several instrument loads may have been destroyed. It is best to check U1 first, or to test Q1 and VR1 outside the instrument and then replace them before reinstalling the A56 -15V Supply board.

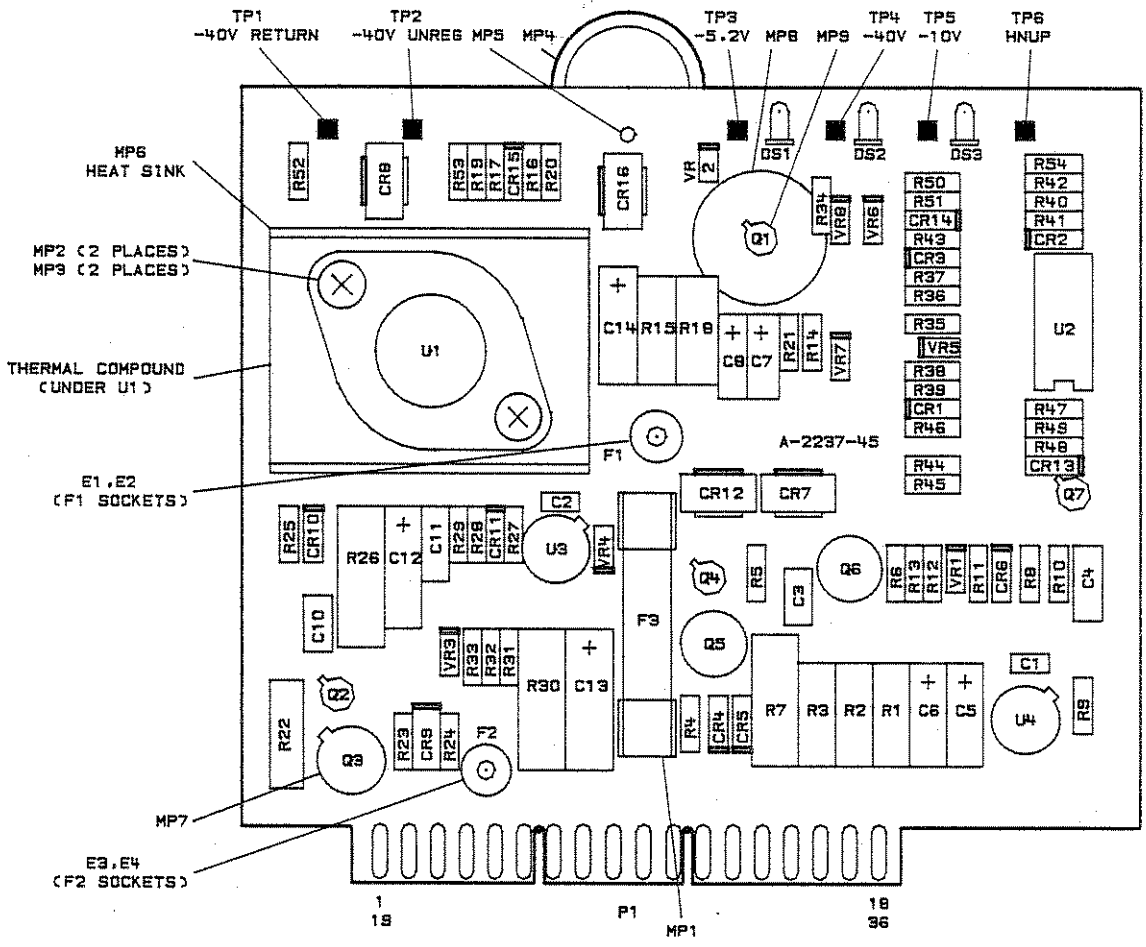


Figure 8-711. A53 Negative Regulator, Component Location Diagram

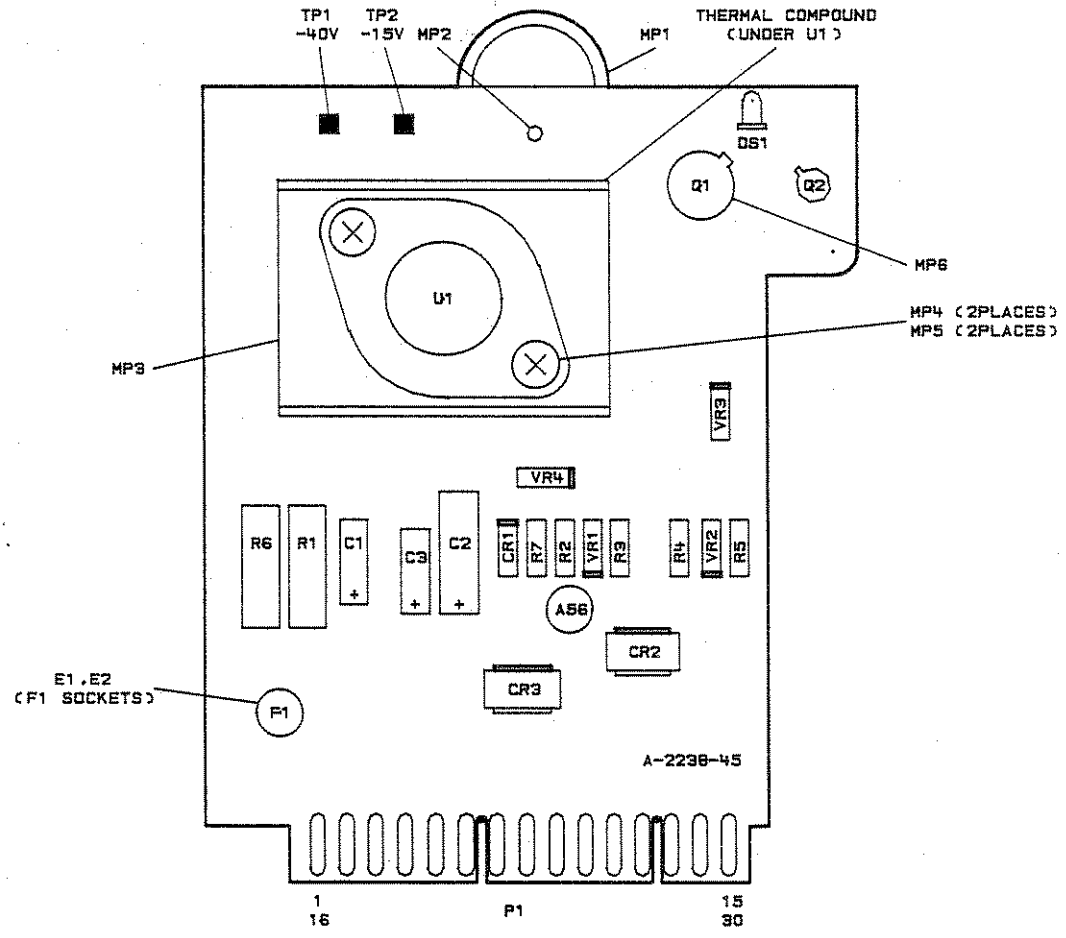


Figure 8-712. A56 -15V Regulator,
Component Location Diagram